ML 2035/2036 application:
Programmable sine wave generator

VHF/UHF TUNER

Microcontroller NiCd charger

AF filter and amplifier

Stereo mixer

Ah meter

MIDI channel indicator

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We regret that owing to unforeseen circumstances 'Low frequency filter' has had to be carried over to next month, when it will be titled 'Output amplifier with AF band-pass filter'.

In next month's issue

- Output amplifier with AF band-pass filter
- Telephone-controlled switch
- The analogue subsystem – Part 3
- 535 board with EPROM emulator
- VHF/UHF TV tuner – Part 2
- Precision clock for PCs
- Power MOSFET tester
- Electronic load resistance
- and others for your continued interest

Front cover
Adding a suitable colour monitor to the tuner described on pp 8–12 forms a complete television receiver. Microprocessor-controlled, menu-driven, with digital tuning, a small LCD screen, optional infra-red remote control, and a memory capacity for up to 100 preset stations, the tuner is also suitable for TV DXing and interfacing to a computer system via a video digitizer. It gives full coverage of the VHF and UHF television bands.

Ampere-hour meter - page 16

Microcontroller-driven NiCd battery charger - page 30

Stereo mixer - page 44

ROM gate switch-over for Atari ST - page 58

ELECTRONICS SCENE

E.A. Newman (b. 1918)

Edward Newman, a pioneer of digital computing, died last August. Shortly after graduating in physics just before the Second World War he joined the EMI Research Laboratories, where he worked with the great Arthur Blumlein.

After the war, he moved to the National Physical Laboratory where he worked with another great, Alan Turing, on developing ACE, one of the world's first electronic computers. It was there that he used his knowledge of television and radar to design digital circuits, which were then revolutionary, but made the project a success.
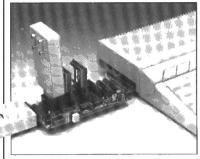
Later, he worked, under A.M. Uttley, on pattern recognition. From then on, he never lost his interest in understanding the human brain and correlating it with computer technology.

J.E. Dingman (b. 1901)

James Dingman, one of the pioneers of satellite communications, died last August. He was chief engineer of the American Telephone and Telegraph Company when, in 1962, he oversaw the first broadcast programme to be beamed into space and back again to earth via Telstar. This satellite (which is still in orbit) launched the modern era of telecommunications.

Many successors to Telstar were launched under Dingman's leadership after he had become Director of Comsat, the Communications Satellite Corporation.

NETWORKING ACROSS ACADEMIA

The computer local area networks (LANs) of around 200 universities, polytechnics and research establishments in Britain have been linked for a decade by JANET, the Joint Academic Network. This system is now being upgraded with the latest high-speed fibre-optic technology, so that, in addition to just carrying messages, it will provide the academic community with an advanced communications infrastructure that will satisfy its needs through to the next century.

To be known as SuperJANET, the improved network is needed to support advanced learning and research activities. These require high-speed data, images and video communications in addition to voice. SuperJANET will augment, but not replace, the existing JANET network that was created in the

early 1980s and which currently serves some 50 000 terminals and provides access to electronic mail services around the world, including the NSFNet (National Science Foundation Net) in the USA.

Higher performance overlay network.
SuperJANET will not change the way that research workers access remote databases and communicatie with their peers in all parts of the world on a routine basis via E-mail. However, it will provide a far higher performance overlay network that will roll out to an increasing number of establishments across the country. Then, as similar networks are developed in other countries, there will be the opportunity of extending the connectivity.

Dr Robert Cooper, who leads the project for the Science and Engineering Research Council/Universities Funding Council joint network team, believes that SuperJANET is unique in Europe – and almost so in the world. Explaining the new network's pioneering role, he added that it will be a test bed, because the academic world is very demanding and will employ the technology before it is widely used commercially.

Britain's Universities Funding Council (UFC) awarded the contract, worth £18 million over four years, to British Telecom (BT). The initial phase will link sites at Cambridge and Manchester Universities, Rutherford Appleton Laboratory, University College London, Imperial College London and Edinburgh University. During 1993-94, around 50 sites will be connected to the network with further ones being added subsequently, subject to additional funding.

Broadband technologies
The network design uses the latest broadband technologies and much of the connectivity will be based on BT's new Switched Multimegabit Data Service (SDMS). Synchronous Digital Hierarchy (SDH) will

become the primary network technology which, together with new broadband switching technologies (distributed queue dual bus and asynchronous transfer mode), will provide for maximum interconnectivity.

Dr Alan Rudge, BT's managing director for development and procurement, with responsibility for all the company's technical research activity, stressed that the advanced broadband switching platform that will interlink sites is vital to industry as well as government and academia. "The SuperJANET contract allows BT to collaborate with universities on new applications which will, in due course, provide business with a competitive edge."

Dr Rudge stressed the need to promote the image that 'broadband is the norm'. He went on to say that BT proposes to participate in collaborative ventures with suppliers to deliver equipment. He further added that there is a need for a critical mass to engender confidence. Hence, BT expects that the availability of the network will provide the vital 'pump priming' function.

Visualization output.
The transmission to Imperial College in London of the visualization output of large-scale computational fluid dynamics calculations performed on the Cray YMP supercomputer at the Rutherford Appleton Laboratory is one engineering application proposed. As the vast amount of data generated by the application can only be absorbed by the user if it is presented as

an image—often with colour and animation—superJANET will obviate the need for the researchers actually to be on the Rutherford site.

Similarly, the Medical Research Council (MRC) Cyclotron Unit at Hammersmith Hospital, in London, has several advanced facilities for producing brain images that are of interest to research workers at other sites. In the pilot project, brain images acquired at Hammersmith will be transferred to the Departments of Psychiatry at Edinburgh University and University College London (UCL) for analysis, and to the supercomputer centre at Edinburgh University for processing.

Interactive video

University College London has facilities to teach surgery via interactive video. Consequently, there is a proposal to set up a series of surgical demonstrations between UCL and the other centres which could support a range of interactive activities including surgical demonstrations from the operating theatre, clinical demonstration in the lecture theatre, discussions between surgical specialists, the co-operative preparation of video teaching material and exploration of ways of using existing courseware designed for self-directed learning in a distance learning environment.

This proposal hasa the support of the departments of surgery at St Mary's Hospital Medical School (Imperial College), London, and the universities of Edinburgh, Glasgow, Manchester and Cambridge.

Applications in the field of information services include library document distribution and an electrical journal testbed as well as a number of applications concerned with transferring large files

rapidly from place to place. The former will aim to demonstrate document request and delivery over the network involving over seven universities (including two former polytechnics) with a view to eventually establishing a regular service between all universities. It will be more cost-effective than the existing inter-library loan arrangements which are slow and labour intensive.

SuperJANET will enable a large variety of tasks—encompassing a number of disciplines—to be undertaken that are currently being held back by lack of a suitable high-speed network. In addition, as each new application is successfully implemented, the benefits of superJANET will become more apparent to an even wider field.

Science and Engineering Research Council, Polaris House, Northstar Avenue, Swindon, England SN2 1ET.

MAPLIN ELECTRONICS NATIONAL KARAOKE CONTEST WON BY SARAH JANE HAVERS

Winner of the Maplin Electronics National Karaoke Contest sponsored by PMI (part of the EMI Music Empire) is Sarah Jane Havers, a back-stage chaperone from

Taplow in Buckinghamshire. Runner-up is Miss Marianne Headington (aged 11) from Little Staughton, Bedfordshire. The judges included Sean King, Editor of *Video & Home Entertainment*, Martin Smith, Head of Programming Picture Music International, Robert Ball, Editor of *Electronics – The Maplin Magazine*, and pop singer Mark Khan. The photo shows Sarah Jane during the two-hour recording session at London's famour Abbey Road Studios, which was the first prize of the contest.

WORLD'S LARGEST QUADRATURE BOOSTER

The world's largest quadrature booster, used to help control the power flow in two parallel transmission lines has successfully completed works tests. The unit, rated at 2000 MVA, 400 kV, has been built at a cost of £5 million by Peebles Power Transformers in Edinburgh for use on Britain's national power grid.

Quadrature boosters are used in conjunction with existing autotransformers to control power flow. They inject a voltage in quadrature to the system phase voltage and variation is achieved by tap changing. Tap changing on the autotransformers injects a voltage that is in phase with the system voltage. Optimum sharing of megawatts and megavars in two parallel circuits can therefore be achieved by a combination of quadrature and in-phase voltage injection.

The largest quadrature booster previously built by Peebles was a 750 MVA, 275 kV unit made up of two core and winding assemblies housed in a single fabricated tank suitable for transportation to site.

The physical size of the latest unit, however, meant that each core and wind-

ing assembly had to be housed in a separate tank. The shipping mass of each assembly at 240 tonnes was in fact greater than the combined shipping mass of the 750 MVA unit.

Following the successful completion of testing, the giant booster has been shipped from Granton Harbour on the Firth of Forth by RoRo (roll-on, roll-off) ship to the port of Goole en route to the National Grid substation at Stockbridge, near Sheffield. **Peebles Power Transformers Ltd, East Pilton, Edinburgh, Scotland EH5 2XT.**

APPLE CHOOSES INTEL FLASH STORAGE CARDS FOR NEWTON MESSAGEPAD

Intel Corporation is providing Apple Computer Inc. with 2 Mbyte flash storage cards packaged in credit-card size for the Newton* Messagepad*.

The many benefits of flash are allowing mobile system designers to make the vision of hand-held computing devices a reality. In designing Newton technology, Apple was able to go beyond the disk drive paradigm. Instead of retrofitting flash to behave like a drive, they looked at the unique benefits of flash and designed a better storage system for their customers. * Newton and Messagepad are trademarks of Apple Computer Inc. **Intel Corporation (UK) Ltd, Pipers Way, Swindon, England SN3 1RJ.**
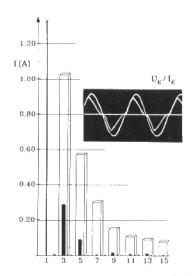
MEGAVISION – A CHIP SET FOR TELEVISION AND MULTIMEDIA

As a successor to its award-winning 'Featurebox 88' chip set, Siemens has introduced a complete system of integrated circuits that not only offers flicker-free television, but can also be used in studio and multimedia applications. Picture quality has been enhanced even beyond the levels offered by 100 Hz technology. New functions have also been implemeted. Changing over to submicron technology has allowed a higher level of integration and this in turn provides cost benefits. The modular component principle starts with picture processing for 16:9 screens and, with the most sophisticated configurations, includes noise reduction, picture-in-freeze frame, freeze frame in picture, nine-element picture with tuner scanning and full-frame mode without line flicker.

LOW-HARMONIC SWITCHED-MODE POWER SUPPLIES

To reduce the harmonic content of switched-mode power supplies for TV sets and monitors, Siemens has developed a set of control chips that conform to tomorrow's standards today. The chips, coded TDA 4061 and TDA 4605, 4605-2, 4605-3, are designed for different power consumptions. Their use produces a sinusoidal current input for the flyback power supplies.

Siemens AG, LZF Infoservice, Postfach 23 48, D-90713, Munich, Germany.

Harmonics |n|

An harmonics analysis based on EN60555 shows the excellent values for switched-mode power supplies that can be obtained with the TDA4605 control chips (black bars). The columns show the permissible limits for the operational data applying here: 230 V a.c., 50 Hz, 1.36 A current input (fundamental), i.e., a power consumption of 300 W. The oscillogram shows the quasi-sinusoidal relationship between the input voltage and input current.

VHF/UHF TELEVISION TUNER (PART 1)

Together with a suitable colour monitor, the television tuner described here forms a complete television set. Microprocessor controlled, menu-driven, with digital tuning, a small LCD text screen, optional infra-red remote control, and memory capacity for up to 100 preset stations, the tuner is ideal for TV DXing and interfacing to a computer system via a video digitizer. The unit offers full coverage of the VHF and UHF TV bands, and apart from the normal mono sound channel, analogue stereo sound as used in some countries on the European continent is also provided.

Design by W. Sevenheck

THE block diagram of the TV tuner is given in **Fig. 1**. The most important sections are the power supply, the (ready-made) VHF/UHF tuner module, and the intermediate frequency (IF) circuit plus sound decoder. A microprocessor core based on a 8751 controller arranges, among others, the control of a two-line LCD text display, a small keyboard, and the tuning of the tuner module. The serial I²C bus is used for the communication between the microcontroller and a number of other ICs in the circuit. The digital signals needed for this communication are generated by the microcontroller itself. In addition, the 8751 also decodes and processes the digital RC5 codes received from an RC5 compatible infra-red remote control.

The TV tuner supplies a colour-video-blanking-synchronization (CVBS, or simply 'composite video'), output signal into a standard load impedance of 75 Ω.

Circuit description

The circuit diagram in **Fig. 2** shows the VHF/UHF tuner module, the sound and vision decoders, and the power supply. Nearly all the 'work' in the circuit is done by three powerful integrated circuits from Philips Semiconductors. All three, the TDA3842 multistandard video IF processor, the TDA3857 sound IF processor, and the TDA8415 sound processor, appear in recommended application circuits as found in the Philips datasheets. Two surface-acoustic wave (SAW) filters from Siemens are used to minimize cross-interference between sound and vision. Both filters pass the down-converted 38.9-MHz reference carrier. Filter Fl₁ also passes the sound component, while Fl₂ does the same with the vision component. In both cases, the 38.9-MHz signal is needed as a reference in the decoding operation. A simple analogue-to-digital converter (ADC) based on a resistor ladder network and an LM339 opamp (IC₄) converts the AFC (automatic frequency control) signal supplied by IC₃ into four logic levels that are accepted by the microcontroller, which uses the 4-bit code to ensure the best possible tuning of the tuner module.

The tuner module, a Type UV816PLL from Philips Components, requires three supply voltages: 5 V, 12 V and 33 V. The unit gives full coverage of the VHF-1 (channels E2 to C; 48.25 MHz to 82.25 MHz), VHF-3 (175.25 MHz to 224.25 MHz) and UHF (channels E21 to E69; 471.25 MHz to 855.25 MHz) TV bands. It should be noted that the VHF-1 and VHF-3 bands are no longer used for television in the UK. They are still of interest, however, because of the many signals that can be received (under favourable propagation conditions) from overseas TV stations transmitting in these bands.

Tuning is accomplished with the aid of (serial) digital commands applied to the module via its I²C bus connections, SDA and SCL. The intermediate frequency signal is available on the two IF outputs, pins 16 and 17. The UV816PLL is provided with a digital programmable phase-locked loop (PLL) tuning system. This enables tuning with a 62.5-kHz raster at crystal accuracy. Apart from tuning, band switching is also carried out via the I²C bus. The tuner's AGC input is driven by the TDA3842 video processor. The video (vision) and audio (sound) decoder circuits are connected in parallel to the tuner's IF outputs.

Vision channel

After the sound information has been eliminated by SAW filter Fl₂, the IF signal is applied to IC₃, a Type TDA3842 multi-standard video IF amplifier/demodulator. The internal structure of this IC is given in **Fig. 3**. Glancing back at the circuit diagram in Fig. 2, it is easily seen that the TDA3842 is used in its standard application circuit. However, the switch marked 'video-off' is not implemented, while the video switch at pin 9 is available as a connection (solder spot) only, which allows the AGC to be driven by negative (B/G) or positive (L) modulation of the sync signal. The B/G option is the default. The L option is only used with TV systems other than PAL, such as

SECAM.

In the following descriptions, frequencies that apply to the UK television standard (CCIR System I) are given in brackets.

A 5.5 MHz (6.0 MHz) sound subcarrier trap is connected between pins 13 and 14 of the TDA3842. The parallel *LC* tuned circuit required for the video demodulator is connected to pins 10 and 11. The demodulator supplies the AFC (automatic frequency control) via a 90° phase shift. The preset potentiometer connected to pin 2 determines the operating point of the AGC. If the signal level is too low, transistor T3 arranges for the mute circuit to be actuated. The audio channel in the TDA8415 (IC2) is then cut off, so that the loudspeaker does not produce noise. The sound channel is opened again when a sufficiently strong signal is received.

The BC547B transistor at the video output of the TDA3842 buffers the video signal, and ensures an output impedance of about 75 Ω. Capacitors C31 and C32 block the d.c. component in the output signal.

The AFC output signal produced by the TDA3842 is fed to the above mentioned 4-level comparator circuit around IC4. The resultant 4-bit code supplied by the four comparator outputs is used by the microcontroller to fine-tune the receiver.

Sound channel

The sound channel is based on two further ICs from Philips Semiconductors' family of high-integration TV/video building blocks. These ICs are the TDA3857 IF amplifier with two FM demodulators, and the TDA8415 sound processor for two-language sound, with integrated filters and I²C bus control. To begin with, the video component is suppressed by SAW filter FI1, while the 38.9 MHz reference carrier and the sound component are passed. Next, the balanced IF signal is applied to IC1.

The internal organisation of the TDA3857 is given in **Fig. 4**. First, the level of the IF signal is 'stabilized' with the aid of an automatic gain control (AGC). The speed of this control is determined by capacitor C1, which is connected to pin 2. The sound intercarrier is restored on the basis of the input signal, while any residual AM signals are suppressed. The two components produced by the mixer, 5.5 MHz (6.0 MHz) and 5.74 MHz, are separated by appropriate external ceramic filters, X6 and X7, and then processed separately in the IC. The 5.5 MHz (6.0 MHz) subcarrier supplies the main sound channel as produced by any mono TV set. The second lim-
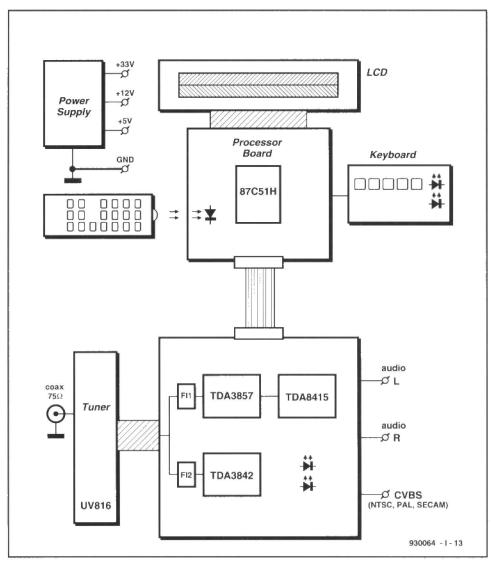
Fig. 1. Block diagram of the VHF/UHF TV tuner. A microcontroller is used to control the analogue sections, while an LCD is useful for operating the tuner.

iter/demodulator in the TDA3857 is tuned to a narrow band around 5.74 MHz, which contains information for stereo or two-language broadcasts. Note that this type of analogue stereo sound with TV broadcasts is used in some European countries only, including Germany and Holland. It is not used in the UK, where stereo TV sound is digital and based on the NICAM-728 standard. Two tuned circuits, X2 and X3, are used to demodulate the sound signals at 5.74 MHz and 5.5 MHz (6.0 MHz) respectively. In the absence of a 5.74-MHz component, the associated sound channel is automatically muted, leaving the main sound channel to be heard only. The two audio signals are output via pins 6 and 7, and fed to the audio processor, IC2. Preset P1 is included in the circuit to allow the level of the two audio channels — 5.5 MHz (6.0 MHz) and 5.74 MHz — to be made equal. This is necessary to ensure the best possible channel separation with stereo broadcasts.

The sound processor, IC2, is a TDA8415. This IC has been developed

for stereo or two-language sound in TV sets and video recorders. As shown in the block diagram in **Fig. 5**, audio signals are applied to the two inputs of this processor: '(L+R)/2' or language 'A' goes to input AF1, and 'R' or language 'B' to input AF2. In this notation, 'L' is the left-hand audio channel in a stereo broadcast, and 'R' the right-hand audio channel. A pilot tone modulated 50% AM on a subcarrier at 54.6875 KHz enables the sound processor to distinguish between stereo and two-language broadcasts. The pilot tone is contained in the signal for the second channel (E2) and has a frequency of 117.4 Hz for stereo broadcasts, or 274.1 Hz for two-language broadcasts. Depending on the mode of the sound processor (mono, stereo or two-language), LED D1 and/or D2 is controlled by IC outputs C1 and C2 via two buffer transistors. The sound processor IC itself is controlled via the SCL and SDA lines that form the I²C bus. Special commands on this bus allow the processor's signal inputs to be selected, and the muting to be actuated. The timing signals
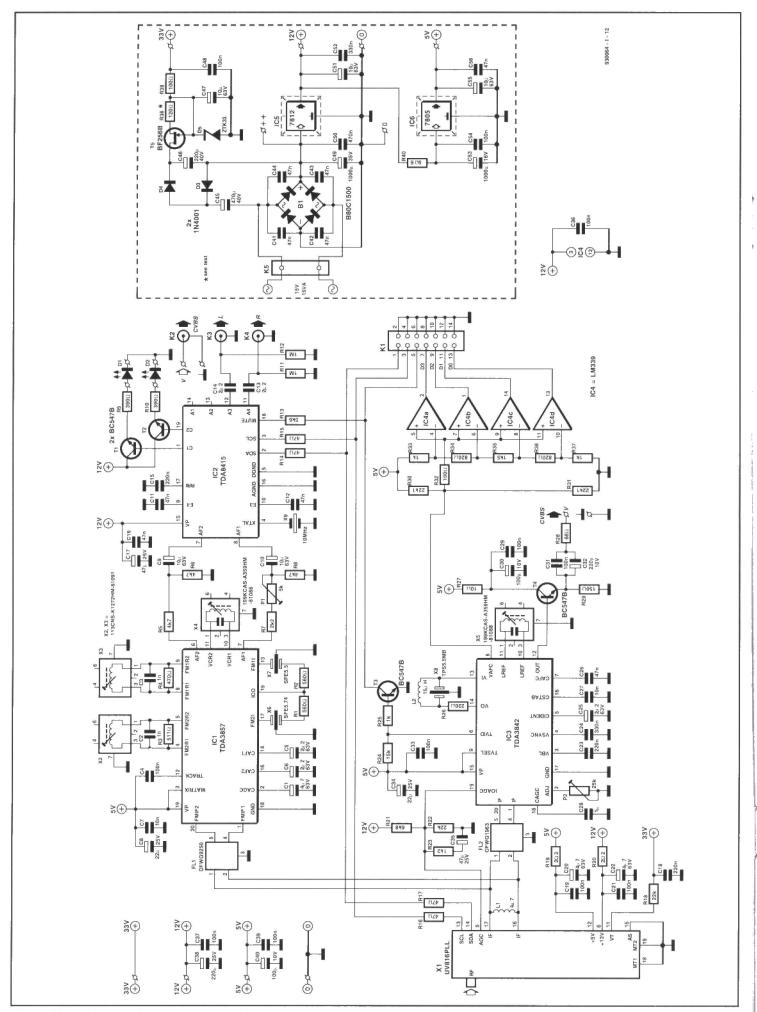
Fig. 2. Circuit diagram of the analogue section and the power supply. The circuit remains relatively simple thanks to the use of three dedicated integrated circuits developed for the modern TV industry.
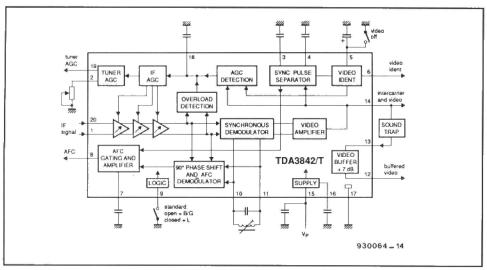
Fig. 3. Block diagram and typical surroundings of the TDA3842 video demodulator (courtesy Philips Semiconductors).
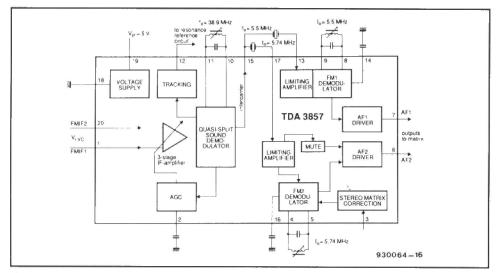
Fig. 4. Block diagram of the TDA3857 sound demodulator (courtesy Philips Semiconductors).
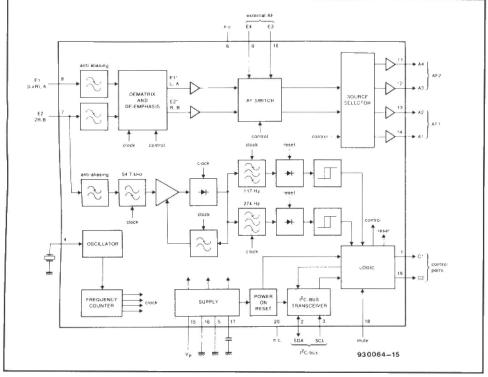
Fig. 5. Block diagram of the TDA8415 audio processor for TVs (courtesy Philips Semiconductors).

required for these operations are derived from a 10-MHz quartz crystal, X9, which is connected to an on-chip oscillator. The audio output signals are fed out of the circuit via capacitors C13 and C14. The additional audio inputs, E3 and E4, and the additional audio outputs, A3 and A4, are not used in the present circuit.

Power supply

All supply voltages required for the VHF/UHF TV tuner are derived from a single 15-V, 15-VA mains transformer, whose secondary winding is connected to K5. A voltage doubler, D3-D4-C45-C46, turns the 15 V a.c. into about 35 V d.c., which is stepped down to a regulated voltage of 33 V by a zener diode, D5, connected to a current source, T5-R38. The regulated and temperature-compensated 33-V supply voltage is applied to the UV816PLL TV tuner module.

The direct voltage of about 18 V across C49 is stepped down to 12 V by regulator IC5. This also powers the second regulator, IC6, which provides the 5-V supply rail. Resistor R40 is connected between the output of IC5 and the input of IC6 to reduce the dissipation of the 5-V regulator.

Traffic control: an 8751

The remainder of the circuit is given in **Fig. 6**. All control activities are assumed by a single microcontroller Type 8751, which comes ready-programmed through our Readers Services. The circuit around the microcontroller has no surprises. The power-up reset network is formed by R2-C2. The 10-MHz clock signal is generated with the aid of crystal X1. Two resistor arrays, R6 and R7, provide the necessary pull-up resistors on a number of I/O lines. The two-line LC display is connected to boxheader K2, which supplies all the necessary drive signals, including the contrast voltage which is set with P1. Jumper JP1 is used to actuate the background light on some types of display unit.

Connector K1 forms the link with the rest of the circuit. Apart from the SDA and SCL signals, this bus also carries the 4-bit AFC information supplied by IC4, and the mute signal, ID.

As already mentioned, the TV tuner has a capacity of 100 preset stations. Since the 8751 does not have enough internal memory for this purpose, external memory has been added in the form of an I^2C compatible EEPROM with a capacity of 256 bytes. The EEPROM, a Type PCF8582A, is capable of retaining data without a backup voltage. An *RC* network, R4-C8, is connected to the PTC input to make sure
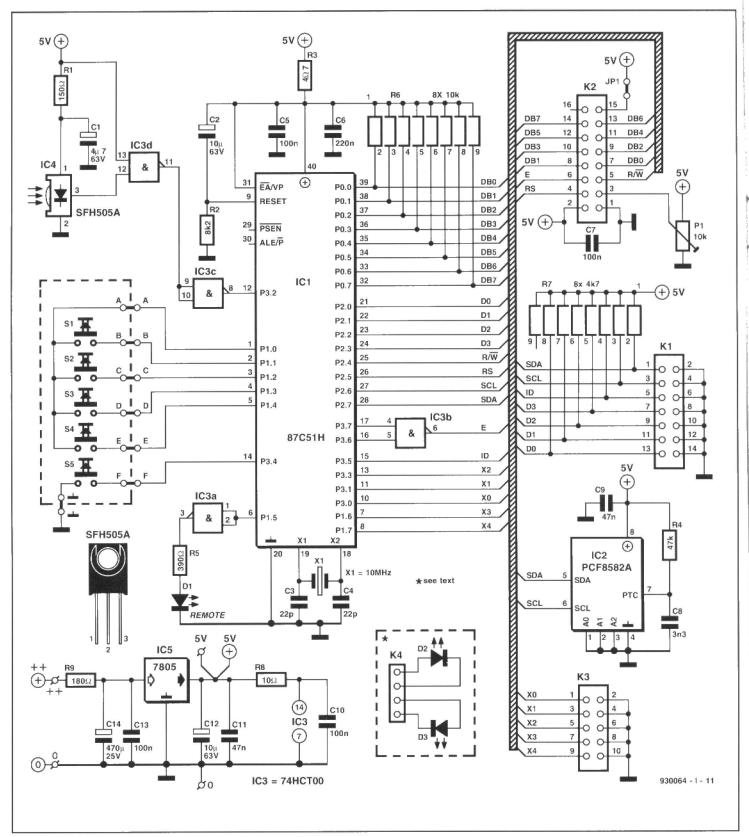
Fig. 6. Circuit diagram of the digital control based on an 87C51 microcontroller from Intel. The preset stations are stored in an EEPROM, IC2.

that the timing of the read/write cycle in the memory is correct.

The local keyboard on the tuner consists of five press-keys which are connected directly to microcontroller port lines.

The infra-red receiver is formed by IC4, an SFH505A module from Siemens. The pulses supplied by the IR receiver reach the microcontroller via inverters IC3c and IC3d. The microcon-troller is programmed to respond to codes transmitted by RC5 compatible (Philips standard) remote control units, and causes LED D1 to flash while a valid IR signal is being received.

Finally, the processor board has its own 5-V regulator to improve the separation between the digital and analogue sections of the tuner. An additional advantage of the separate supply is that the processor board may be used for other applications. In this regard it is useful to mention connector K3, which carries the non-used I/O lines.
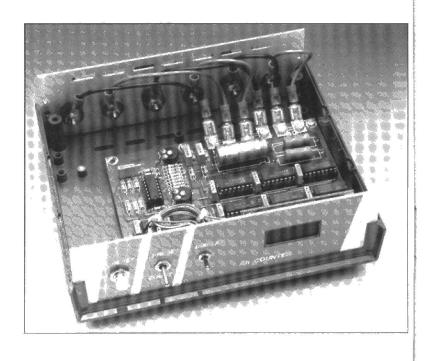
Next month's second and final instalment of this article will discuss the construction of the printed circuit boards, and the enclosure in which the tuner is fitted. Also, the operation of the unit will be discussed extensively.

Ah METER WITH DIGITAL DISPLAY

Design by K. Bachun

Knowing the current drawn (by a battery) or generated (by a solar cell) over a period of time is a requirement in many applications that can be met with the meter described in this article.

The product of current and time is a measure of the electric charge that has been transported in a circuit. It is usually measured in ampere hours (Ah = 3600 coulomb). It must not be confused with power, which is a product of current and voltage. An instrument that measures ampere hours is of interest, for example, in assessing the effectiveness of a solar battery. Normally, it is not accurately known how much charge the solar cells generate nor how much the load connected to the battery needs. The present meter can become a permanent part of such a setup or be used in the design stage to measure both quantities. It indicates these on a three-digit LED display.

Principle of measurement

The principle of operation is shown in the block diagram of **Fig. 1**. A low value resistor has been introduced in the circuit between the solar cell and battery charged by this cell. The potential drop (pd) across this resistor caused by the charging current (from the solar cell) or the discharge current (through the load) is evaluated by the Ah meter.

The pd is applied to two differential amplifiers, whose output voltages would be equal but 180° out of phase (that is, inverted with respect to one another), if the input were not a simple supply voltage. Thus, the adder amplifies only one voltage; the other (which, with a symmetrical supply, would be negative) is nil. The output of the non-reactive adder is, therefore, a voltage that is proportional to the current and which is used to drive a voltage-controlled oscillator (VCO – also called voltage-to-frequency converter).

The VCO generates rectangular pulses whose frequency is proportional to the current. The pulses are divided and counted, and then used to drive an LED display.

Since the polarity of the drop across the shunt resistor shows whether the pd is caused by a charging current or a discharge current, the output of a differential amplifier also shows the direction of the current. The output can thus be used to indicate the direction of counting. When energy is drawn from the battery, the counter counts downward; when the battery is being charged by the solar cell, it counts upward.

The meter does not in any way control or affect the charging current; this can be done only by a special solar charging regulator.

The display does not show the state of charge of the battery to the nearest millampere second, since self discharge and temperature dependence of the battery are not taken into account.

The circuit

The battery, solar cell and load are connected to the circuit in **Fig. 3** by heavy duty connectors. The shunt resistor between battery and cell is formed by two parallel power resistors, R_{46}-R_{54}. If the maximum value of the current is assumed to be 10 A, the drop across the shunt resistor is 0.5 V. If the value of the shunt resistor were higher, the drop would be unacceptably
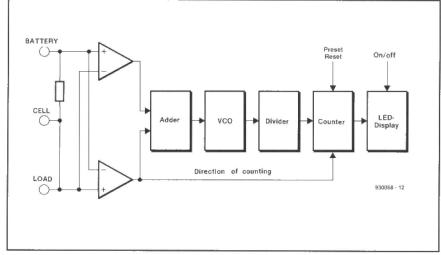
Fig. 1. Block diagram of the Ah meter.
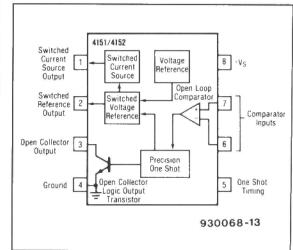
Fig. 2. Circuit of the RC4151 (IC_8).
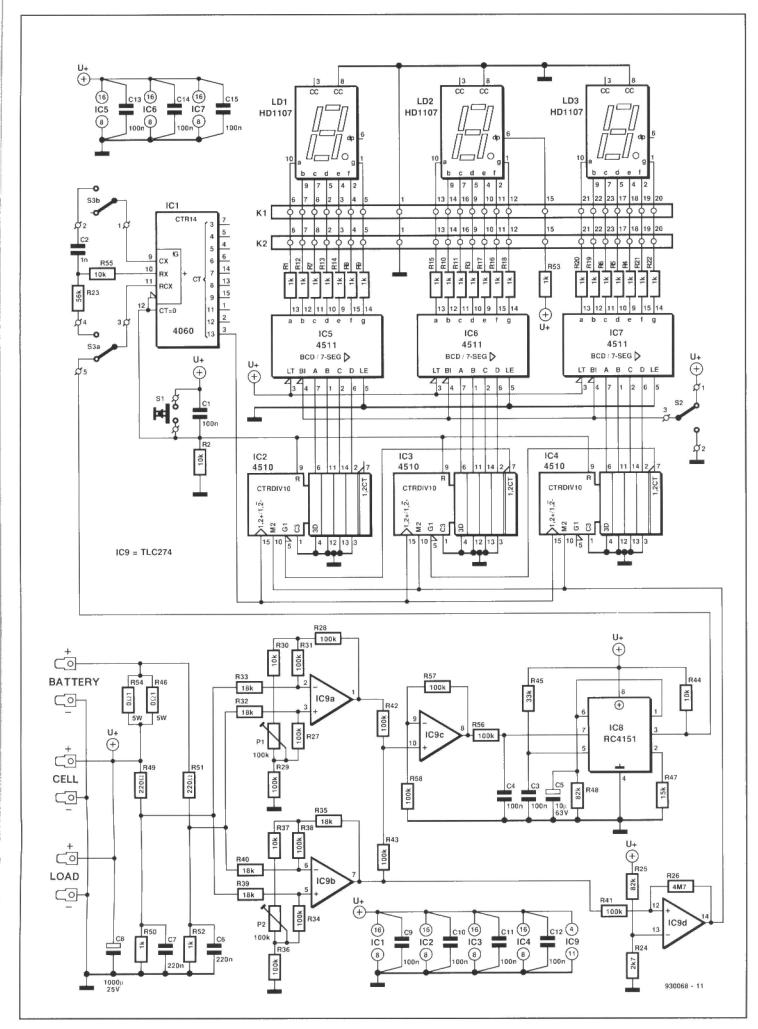
Fig. 3. Circuit diagram of the Ah meter.
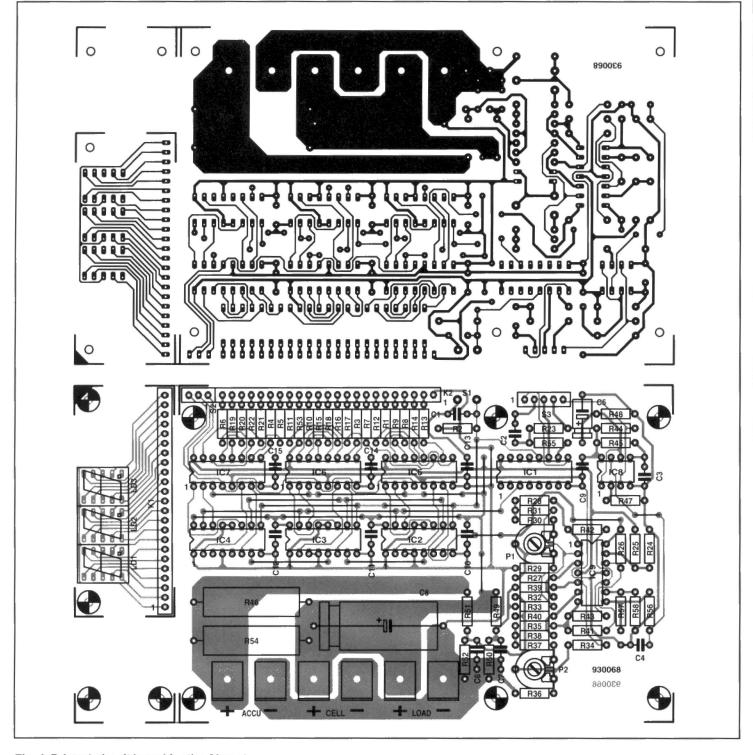
Fig. 4. Printed-circuit board for the Ah meter.
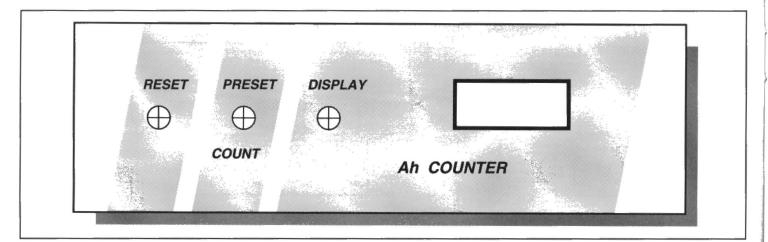
Fig. 5. Front panel foil for the Ah meter (see page 70).

high.

Potential dividers R_{49}-R_{50} and R_{51}-R_{52} reduce the common-mode voltage by about a fifth, so that the unregulated supply voltage which the meter draws from the battery or solar cell is always a little higher than the input voltage at one of the differential amplifiers. If the supply voltage is regulated, it is imperative that the differential input voltage, which in the present design is only four fifths of the drop across R_{46}-R_{54}, that is, not more than 400 mV, cannot exceed the common-mode range of the opamps.

The accuracy of the measurement is not affected by the variable supply voltage, as long as this lies within the usual range of 10-14 V. By the way, the Ah meter cannot be used with 24 V cells and batteries.

Capacitor C_8 smooths the charging and

Fig. 6. Completed prototype without enclosure.

PARTS LIST

Resistors:
R_1, R_3-R_{22}, R_{53} = 1 kΩ
R_2, R_{30}, R_{37}, R_{44}, R_{50}, R_{52}, R_{55} = 10 kΩ
R_{23} = 56 kΩ
R_{24} = 2.7 kΩ
R_{25} = 22 kΩ
R_{26}-R_{29}, R_{31}, R_{34}-R_{36}, R_{38}, R_{41}-R_{43},
R_{56}-R_{58} = 100 kΩ
R_{32}, R_{33}, R_{39}, R_{40} = 18 kΩ
R_{45} = 33 kΩ
R_{46}, R_{54} = 0.1 Ω, 5 W
R_{47} = 15 kΩ
R_{48} = 82 kΩ
R_{49}, R_{51} = 2.2 kΩ
P_1, P_2 = 100 kΩ preset potentiometer

Capacitors:
C_1, C_3, C_4, C_9-C_{15} = 100 nF
C_2 = 1 nF
C_5 = 10 µF, 63 V
C_6, C_7 = 220 nF
C_8 = 1000 µF, 25 V

Integrated circuits:
IC_1 = 4060
IC_2-IC_4 = 4510
IC_5-IC_7 = 4511
IC_8 = RC4151 (Raytheon)
IC_9 = TLC274

Miscellaneous:
S_1 = SPST switch
S_2 = spring-loaded, press-to-make switch
S_3 = double-pole, change-over switch
LD_1-LD_3 = HD1107
6 off 10 A, banana socket for chassis
    mounting*
6 off car-type spade terminal (male and
    female) for PCB mounting*
2 off 23-way terminal strip, male
Enclosure, as required
PCB No. 930068 (see p. 70)
Front panel foil No. 930068F (page 70)

* either of these are required, see text.

supply voltages so that voltage peaks cannot cause spurious measurements. Capacitors C_6 and C_7 short out any short spurious pulses at the inputs of the operational amplifiers.

The design of the differential amplifiers is traditional. Their amplification is about ×20, which gives a peak output voltage of around 8 V. The value of the resistors at the non-inverting inputs corresponds to that of the resistors at the inverting inputs. The common-mode rejection of a differential amplifier relies on the equality of these resistors. To avoid the necessity of costly close-tolerance resistors, the amplification factors can be adjusted with P_1 and P_2. This also serves another function. It is well known that a battery must be charged with 40% more energy than can be drawn from it. If, for instance, it has been charged with a quantity of electricity of 1 Ah, only 715 mAh can be drawn from it. This means that the amplification of IC_{9a} must be 1.4 times as large as that of IC_{9b}.

As explained earlier, the polarity of the drop across the shunt resistor causes IC_{9a} to amplify when the battery is being discharged, and IC_{9b} when the battery is being charged. The output of the non-amplifying opamp is 0 V. Since both outputs are connected to the high-impedance, non-inverting (+) input of IC_{9c}, potential divider R_{42}-R_{43} functions as if it were connected to ground. This means that the amplification of IC_{9c} is ×2.

The output of IC_{9b} is also applied to Schmitt trigger IC_{9d}. As soon as the output of IC_{9b} reaches a certain level, IC_{9d} changes state (goes high). The output of IC_{9d} determines the direction of counting

of IC_2-IC_4.

Reverting to the output of IC_{9c}, this voltage, which is directly proportional to the charging/discharge current, is applied to voltage-controlled oscillator (VCO) IC_8—see **Fig. 2**. The output of the comparator in this circuit drives a monostable multivibrator (MMV), which in its turn controls the switched current source, the switched voltage reference and the open-collector logic output transistor. When the voltage at pin 7 of IC_8 exceeds that at pin 6, the comparator changes state and triggers the MMV. This stage then enables the current source, the voltage reference and the output transistor. It operates basically in the same way as the well-known Type 555 timer, in that it charges a capacitor (C_3), which is connected to $U+$ via R_{45}. The capacitor voltage is monitored at pin 5; as soon as this reaches 67% of the supply voltage, the mono time is terminated, upon which the capacitor is discharged immediately via a transistor.

During the mono time, the current source provides a current at pin 1 that is directly proportional to the reference voltage and external resistor R_{47}. The switched voltage reference provides a potential of 1.9 V at pin 2, which is equal to fixed internal reference voltage. The open-collector transistor connects the output (pin 3) to ground. In other words, during the mono times, the switched voltage reference generates a positive voltage pulse; the current source generates a current pulse that is well defined in duration and amplitude; and the output transistor has transmitted a logic pulse that is compatible with most logic cards. All these signals are directly pro-

---

portional to the level of the input voltage. When the mono time elapses, these three functions are disabled.

Circuit IC_8 operates here in a standard application. The output of IC_{9c} is applied to the non-inverting input of the comparator (pin 7) via a low-pass filter, R_{56}-C_4. The MMV operates as an oscillator since it is continuously triggered by the common-mode input voltage. The current source provides a current of $U_{ref}/R_{47} = 40\,\mu A$ for a time $1.1 \cdot R_{45} \cdot C_3 = 3.63$ ms into integrating network R_{48}-C_5. Critical is the feedback of the integrator to the inverting input of the comparator (pin 6), which raises the pulse repetition rate until the average potential across the integrator is equal to the common-mode voltage at pin 7. The average voltage at pin 6 is directly proportional to the output frequency (and that at the open-collector output) since the quantity of charge in each current pulse is accurately controlled. In other words, the output frequency is directly proportional to the input voltage.

The external components determine the design parameters. The time constant of the output signal is the product of the mono time, the amplitude of the output current at pin 1, and the reciprocal of the current through the integrating resistor. From this, the formula for the output frequency, f_0 is

$$f_0 = (U_{ref} / R_{47} \cdot R_{48} / U_{in} \cdot 1.1 \cdot R_{45} \cdot C_3)^{-1}.$$

With component values as specified, this yields an output frequency of 212 Hz. This will be reverted to later on.

If any component values are altered, it should be noted that the value of R_{47} must be between 12 kΩ and 20 kΩ. Also, because

of the offset of the operational amplifier, it is not possible to obtain an input voltage of exactly 0 V. It does not pay to compensate the offset, because IC_8 in its standard configuration operates correctly only from 10 mV onward in any case. The consequent error of 2 Hz (equivalent to <1% of full-scale deflection) is negligible compared with, for instance, that caused by the self discharge of the battery.

The output of the voltage-to-frequency converter is applied to divider IC_1 via switch S_3. Divided by 2^{13}, it is output at pin 13 and applied to cascaded CARRY OUT /CARRY IN binary-coded decimal (BCD) counters IC_2–IC_4. Pressing S_1 sets the counters (and the divider) to 0. Note that R_{23}, R_{55}, and C_2 serve no useful function in normal operation.

The counting direction inputs of IC_2–IC_4 are driven by IC_{9d}. Note that the preset inputs are not used. The outputs of the counters are fed to BCD-to-7-segment decoders IC_5–IC_7. The decoders control the 7-segment LED displays LD_1–LD_3.

During normal operation, the displays are not on, since the Bl(anking) inputs of the decoders are at ground potential via S_2. It is advisable to use a spring-loaded switch here, so that the display cannot be left on inadvertently. Note that the right-hand decimal point is always on, however, to show that the meter is functioning.

To ensure that the display increases from 00·0 to 10·0 when a constant current of 10 A has flown for 1 hour, the counters need 100 pulses per hour or 100/3600 pulses per second. This means that the VCO must generate a signal at a frequency of $100/3600 \cdot 2^{13} = 227.56$ Hz. Working back, this means that the VCO needs an input

of 8.58 V. Since the differential input voltage is fairly accurately 410 mV when a current of 10 A flows through the shunt resistor, the differential amplifier must have an amplification of 8.58 / 0.41 = 20.9.

Owing to component tolerances and other imponderables, the potentiometers should be preset empirically. This is done by connecting the positive output of an accurate 500 mV source to the '+ battery' terminal, and the negative output to the '+ cell' terminal. Turn P_2 until a frequency counter at the output of (pin 3) of IC_8 shows 228 Hz. Then reverse the connections of the voltage source and adjust P_1 until the display reads 1 / 1.4 · 228 = 163 Hz.

The display is checked by switching into circuit (with S_3) components R_{23}, R_{55}, and C_2. This actuates an RC oscillator in IC_1. If everything is all right, the display will fairly quickly give a high reading. This position of S_3 is also for presetting a given counter state when, for instance, the Ah meter is connected to a fully charged battery.

Construction

The printed-circuit board in **Fig. 4** can, if desired, be cut into two to enable the displays to be mounted at an angle behind the front panel. Otherwise, fit them in IC sockets so that they protrude above the other components. The 23-way terminal strips, K_1 and K_2, must be used in both cases.

Use car-type insulated spade terminals (male and female) for 'battery', 'cell' and 'load'. If, however, the meter is given its own enclosure, use the 10 A chassis-mounted banana sockets specified in the parts list. **END**

FUZZY LOGIC MULTIMETER
(PART 2)

There is little to say about the true-r.m.s. converter. The circuit diagram (Fig 5) shows a standard application of the AD736JN, connected to a non-critical R-C network, C4-R15, and three electrolytic capacitors (also uncritical), C5, C6 and C7. The bandwidth of the true-r.m.s. converter exceeds that of the multimeter IC input by far. In fact,

the multimeter IC limits the –1%-bandwidth of the DMM to about 300 Hz. Keep this in mind when measuring signals with a lot of distortion (i.e., containing many higher harmonics), because for the measurement to be accurate, the strongest harmonics have to fall within the 300-Hz bandwidth of the DMM.

The multimeter power supply is relatively simple, consisting essentially of a 5-V regulator, IC10, and an inverter, IC3. Jumpers JP16 and JP17 are remnants of the experimental phase of the circuit, and determine where the analogue and digital ground are interconnected. On the final design of the printed circuit board, JP16 is a

Register Map of Output Data

ADDRESS OR REGISTER NUMBER	REGISTER NAME	REGISTER CONTENTS			
0	Ones	Conversion Result BCD data for least significant digit (The undisplayed digit used fot digital autozero)			
1	Tens	BCD data of Conversion Result (Least significant displayed digit)			
2	Hundreds	BCD Data of Conversion Result			
3	Thousands	BCD Data of Conversion Result			
4	10 Thousands	BCD Data of Conversion Result			
5	Status	D3 Always 1	D2 Latches Continuity	D1 Holding	D0 Low Battery

Register Map of input Data

ADDRESS OR REGISTER NUMBER	D3	D2	D1	D0
0	Hold	High Frequency	Beeper ON	Sleep
1	10^{-0}	Filter Short	$\div 5$	50Hz
2	10^{-4}	10^{-3}	10^{-2}	10^{-1}
3	DC	Ext AC	Divider Sense	Ohms R/2
4	Current	X2	Read Zero	Filter On

BIT SET	VOLTAGE RANGE	OHMS RANGE
10-0	400mV	4M and 40M
10-1	4V	400 kΩ
10-2	40V	40 kΩ
10-3	400V	4 kΩ
10-4	4000V	400 Ω

MEASUREMENT RESULT	BCD DATA
+40000	40000
–	–
+00100	00100
–	–
+00001	00001
00000	00000
–00001	99999
–	–
–40000	60000

FILTER ON	FILTER SHORT	FUNCTION
1	0	Normal filter on condition
1	1	Filter on, RFILTER1 is bypassed. Use this bit combination to compensate for the higher source impedance of the 4V range.
0	1	Bypasses the Filter.
0	0	Invalid combination, do not use

Table 1. Overview of data contained in the MAX134 registers.

A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	PC address line
R4	R3	K0 - K7										R2	R1	R0	MicroSystem
card register address	card address		PC I/O address									register address MAX134			

R4	R3	R2	R1	R0	read	write
0	0	0	0	0	units	input data (see table 1)
0	0	0	0	1	tens	input data (see table 1)
0	0	0	1	1	hundreds	input data (see table 1)
0	0	1	0	0	thousands	input data (see table 1)
0	0	1	0	1	status	not used
0	1	x	x	x	data IC9	not used
1	0	x	x	x	data IC4	not used
1	1	x	x	x	not used	not used

Table 2. Addressing standard adopted for the MicroSystem bus/DMM card combination.

jumper, and JP17 must never be fitted. That leaves JP14 in the power supply section. JP14, together with JP10 on the PC interface board, selects the source of the supply voltage. The available options are: (1) the computer's 12-V supply, (2) an external 12-V supply connected to K2 on the interface board, or (3) an external power supply connected to the DMM board (between points U_x and 0).

The design of the digital output section is simplicity itself. Data is clocked directly from the databus into two eight-bit registers, IC4 and IC9. The clock signal is supplied by address decoder IC6, which is controlled by register address lines R3 and R4 (more about this further on). Six bits of IC9 are reserved for internal use. The first bit (pin 19), is used as a software-controlled interrupt enable switch. Thus, the interrupt generated by the DMM on completion of the conversion cycle may be blocked (disabled) either by removing JP13, or by setting the first bit in IC9. If this bit is at 0, NAND gate IC5b no longer feeds the EOC (end-of-conversion) signal supplied by IC1 to transistor T1. The second bit is used to control a LED, D6, which forms a 'software activity' indicator and has, strictly speaking, nothing to do with the function of the DMM card. As long as the LED flashes, you are assured that the PC is talking to the DMM card.

The remaining bits in IC9 are all fed to driver IC11, which is capable of handling far more output current than the average HCT gate. Four bits are used to control relays in the multimeter's input circuit. These bits are also suitable for controlling bistable relays, which have two coils. The advantage of a bistable relay is that it has to be energized only to switch over the contacts, which automatically remain in the new position. This means that a bistable relay does not require a con-

stant current to keep its contacts in a certain position. The advantage is obvious: reduced current consumption. Unfortunately bistable relays are still relatively expensive as well as hard to find as one-offs, and that is why normal, monostable, relays appear in the components list. The control software also assumes that monostable relays are used.

The inputs of drivers 7 and 8 in IC11

may be connected in parallel with driver 6 or 5 by fitting jumper JP11 and JP12 respectively in position 'A'. The parallel connection is useful where two lines are always controlled simultaneously under the control of one bit at one address. If jumpers JP11 and JP12 are set to position 'B', drivers 7 and 8 are controlled separately via two bits of IC4.

The DMM chip, IC1, is controlled via latch IC7 and databus buffer IC8. It was already seen from Fig. 4 that the register addresses of IC1 have to be stable quite a while before data can be read or written. This is achieved by the following trick. Each time a register is addressed in IC1 (R2/R4=00$_B$), address decoder IC6 clocks the register address (R0/R1/R2) in latch IC7. If the desired register address is read first, and the data simply forgotten, the latch will ensure that the address remains stable on the address inputs of IC1. After 3.5 µs, the same register may be addressed again, and data may be read or written.

Address decoder IC6 has a crucial function in the write and read actions to and from the card. It is enabled via the PC interface by the strobe signal and one of the card selection lines en-

COMPONENTS LIST

DMM BOARD

Resistors:
2	1kΩ 0.1%	R1;R5
2	10kΩ 0.1%	R2;R6
1	100kΩ 0.1%	R3
1	1M1 0.1%	R4
2	301kΩ 1%	R7;R8
1	1M2 1%	R9
1	1M 1%	R10
1	10MΩ 1%	R11
1	332kΩ 1%	R12
2	10kΩ	R13;R14
1	22MΩ	R15
2	1Ω5	R16;R21
1	2Ω2	R17
1	1kΩ2	R18
1	2kΩ2	R19
1	1Ω 1%	R20
1	3kΩ3	R22
1	4kΩ22 1%	R23
1	5kΩ11 1%	R24
1	100kΩ multiturn preset	P1

Capacitors:
1	4nF7 MKT	C1
2	22nF	C2;C3
9	100nF	C4;C9;C10; C12;C13;C15; C16;C18;C19
1	33µF 16V radial	C5
5	10µF 16V radial	C6;C7;C8;C17; C25
1	22µF 16V radial	C11
1	10pF	C14
4	100µF 16V radial	C20-C23
1	1pF	C24

Semiconductors:
4	BYV27-100	D1-D4
1	ICL8069C	D5
1	LED, red, high-efficiency	D6
1	BC547B	T1
1	MAX134CPL	IC1
1	AD736JN	IC2
1	ICL7660CPA	IC3
1	74HCT08	IC5
1	74HCT138	IC6
3	74HCT574	IC4;IC7;IC9
1	74HCT245	IC8
1	7805	IC10
1	ULN2803	IC11

Miscellaneous:
1	Passive AC buzzer	Bz1
1	Multifuse 0.4A/50V	F1
1	14-way box header, angled	K1
1	34-way header, angled, side latches	K2
1	PTC max. 2kΩ	PTC1
1	32.768kHz crystal	X1
2	V23042-A1001-B101 relay (Siemens)	Re1;Re2
1	Printed circuit board plus software; order code 920049-1 (see page 70)	

The control software is also available separately: order code 1721 (see page 70)
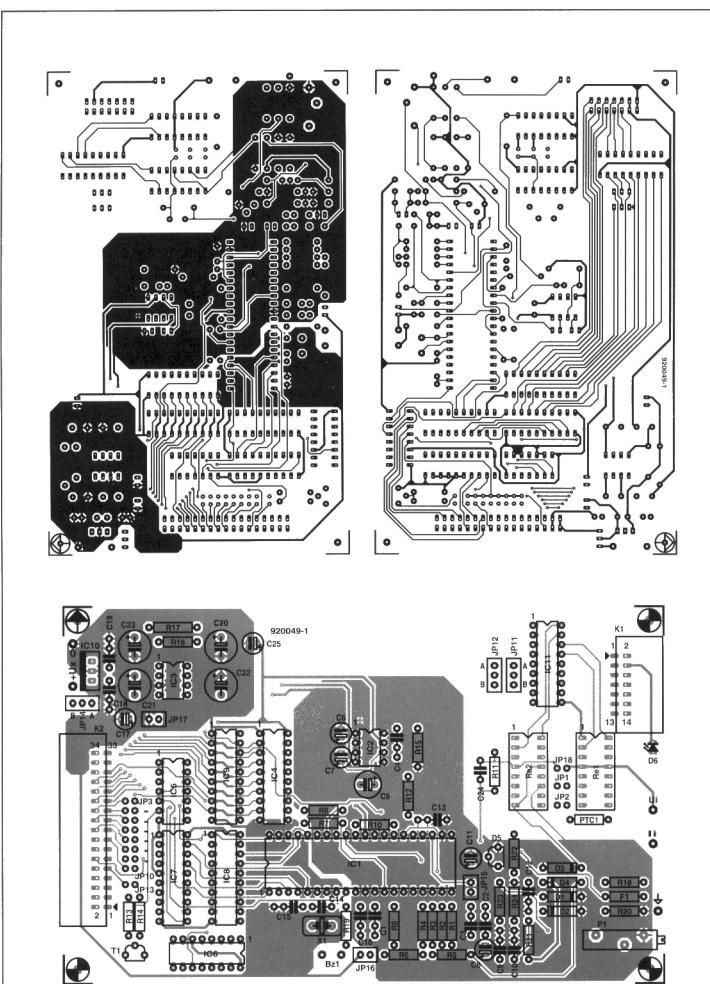
Fig. 6. Track layouts (reduced to 80% of true size) and component mounting plan for the DMM board.
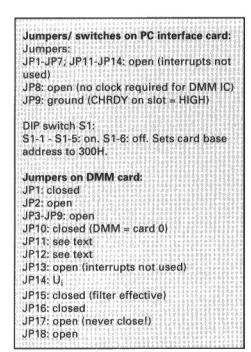
Table 3. Default settings of the jumpers and the DIP switch.

abled via jumpers JP3-JP10. IC6 accomplishes the final addressing with the aid of lines R3, R4 and write. Together with R0, R1 and R2, this gives the addressing shown in Table 2.

The final section of the multimeter circuit to be discussed is the measurement circuit around IC1. The components vital for correct measurement results are resistors R1-R6 and R11, since they determine the resistance and voltage ranges. Unlike R1-R6, R11 is a 1% resistor. A 0.1% type would, of course, be preferred, but proved unobtainable for the value required (10 MΩ). Fortunately, the error (if any) introduced by the higher tolerance on R11 is compensated by calibration preset P1. Tolerance compensation is not available for R1-R6, so any deviation from the stated resistance values causes inevitable differences between the ranges. These differences are kept to a minimum by using 0.1% resistors.

Nearly all switches required for switching between the various ranges are available in IC1. There is, however, one exception. To be able to use the meter as an ohmmeter, the input circuit has to be modified. Junction R1-R2-R5-R6 is usually connected to ground via relay contact Re2. For resistance measurements, R11 has be connected to this junction also. This is achieved by energizing Re2. The junction is then also connected to the 400-mV input of IC1 via PTC1. Together with diodes D3 and D4, the PTC protects the ohmmeter against high voltages (sparks and discharges) at the input terminals. To make sure that the PTC can not affect the lowest resistance range, its value may not be smaller than 2 kΩ under normal cir-

cumstances. Finally, for resistance measurements, input terminal U$_i$ has to be connected to the 400-mV input. This is accomplished by relay Re1, which is also used to connect Ui to the 400-mV input to create the 400-mV range of the multimeter. Jumpers JP1 and JP2 are intended to adapt the input circuit to different types of relay. In most cases, JP1 will be fitted. Jumper JP18 allows relays Re1 and Re2 to be shunted (in which case the relays may be omitted), which forfeits the resistance measurement function of the DMM, leaving the current and voltage (both AC and DC) only. Omitting the ohmmeter function is an option where resistance measurements are not required anyway.

Construction

The artwork for the DMM board (double-sided, through plated) is shown in Fig. 6. Like the PC interface card, this board is available ready-made through the Readers Services. Although construction is straightforward, great attention should be paid to neat and accurate solder work. Remember, one bad solder joint at a crucial point may reduce the accuracy of the meter considerably.

Important notice: although the DMM IC has a 4,000-V range, the printed circuit board is **not** suitable for such a high voltage. This range is, therefore, not available in software. If you write your own software for this circuit, you must not attempt to use the 4,000-V range. The PCB can withstand the mains voltage (220 or 240 V), but always check if the ground of the PC is separated from the mains earth. If the two are connected, swapping the live and neutral lines, although unlikely given their fixed positions on UK style mains plugs and sockets, may cause a short-circuit with disastrous results.

For the time being, preset P1 may be set to the centre of its travel. If you wish, you may want to adjust it for 655 mV measured with a voltmeter. However, before you can start testing the two boards, make the bus cable, and fit the jumpers. The standard jumper settings are given in Table 3. Settings other than the ones shown must be communicated to the program (this is explained in the help texts).

The construction of the 34-way flatcable is simple — see Fig. 7. Although a maximum length of 1 m is indicated, our prototypes gave no problems with cables of up to 1.5 m long. Both cable ends are fitted with an IDC (insulation displacement) socket. If you intend to use more than one DMM card, additional sockets may be pressed on to the cable as illustrated in Fig. 7. The
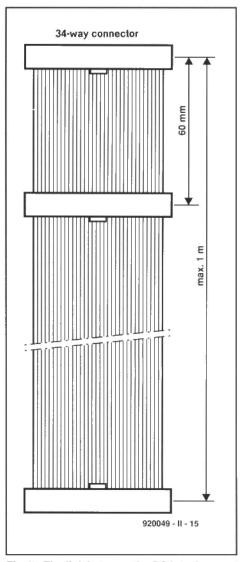
Fig. 7. The link between the PC interface and the I/O card is a bus formed by a length of flatcable. The number of connectors pressed on to the cable depends on the number of cards you wish to connect.

distance between the sockets should be about 6 cm. Finally, check the continuity of all 34 connections.

Software

The DMM does nothing without the appropriate software. Fortunately, this is available on a diskette for IBM PC-ATs (and up) running under MS-DOS. The control software package is called 'Fuzzy Control One', and has been produced by MicroSource. The introduction version of this program is available through our Readers Services, while the full version may be obtained from MicroSource only. As already indicated by its name, the program is tailored to developing control systems using fuzzy logic (Ref. 1). In spite of the designation 'introduction version', all features are available for use — more about this in next month's concluding instalment of this article.

For now, the part of the program that contains the multimeter software

is of interest. Originally, the multimeter was intended as an aid in setting up fuzzy logic control systems. It grew, however, into a fully fledged measuring instrument.

The GUI creation routines are the only ones actually used from the 'LabWindows' package to develop the Fuzzy Control One software. Attention: LabWindows has nothing to do with MicroSoft Windows! Our thanks are due to National Instruments for allowing us to put Fuzzy Control One on floppy disk without having to raise a licence fee for every user. This means that the Fuzzy Control One software is not dearer than most other programs sold through our Readers Services.

It can not be denied that Fuzzy Control One, despite being an 'introduction version', is a very complex program, which requires quite a bit of getting used to. The range of settings and options offered by the program to implement a fuzzy logic control system is staggering, and make the program one of a kind. Documentation is not lacking, either: the total size of the help files alone would easily fill all the pages of this magazine! Incidentally, the help files can be printed, so a manual is readily produced.

A couple of batch programs containing useful examples are supplied to get you going. One of these files, DVM.BAT, launches the multimeter software. Installation is easy: simply start the INSTALL batch, and follow the instructions. After installation, the program always shows the help text when the multimeter is started. This can be turned off by quitting the multimeter and returning to the main menu. Select 'preferences'* from the 'Miscellaneous' menu. After quitting the help text on this part of the program you can turn off the option 'start with help'. To save this setting, store it in the file DVM.FZH. This is done via the 'files' and 'save hardware settings' menus.

The main menu also has an option called 'print data', which enables you to produce hard copy of the help texts (first, however, ascertain the printer port in the same menu).

After starting the multimeter program, you are eventually presented with a screen that contains the following information: current measurement value, average value measured over a predefined number of samples (both values are displayed numerically in a graph), the set measurement range, the type of measurement, the number of measurements used to compute the average ('filter length'), and a histogram that shows the variance of the measurement values contained in the
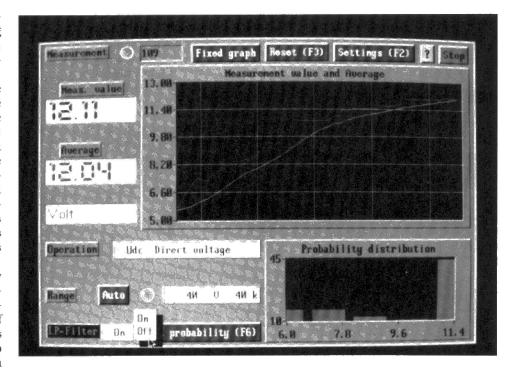
Fig. 8. It is the DVM software contained on the Fuzzy Control One diskette that turns the combination of the DMM card and the PC into a digital multimeter with some astounding functions. Routines from LabWindows handle the graphics presentation of the measurement data, affording ease of program operation (using the mouse).

filter, or in a memory containing 100 measurements. In this way, you obtain information on the measurement value proper, its trend and stability. A number of meter settings can be changed by pointing the cursor at the relevant button and clicking on it. One button determines the rate of zero measurements performed by the instrument. This is necessary to compensate the internal offset of the DMM chip. The software has to deduce the result of the zero measurement from the current measurement value to obtain the real value. Another setting made via this window is 'software calibration', which allows the scale of the DMM to be adapted without having to redo the calibration of the DMM card itself.

The 'preferences' menu also allows you to select the mains frequency (50 Hz or 60 Hz). As already discussed, the reference voltage on the DMM board depends on this frequency, and it is vital to make the selection equal to the mains frequency used in your country. If the set mains frequency is changed, the DMM card has to be calibrated again.

Calibration

Once you have familiarized yourself a little with the control software, the meter is ready for calibration. For some applications it is sufficient to set P1 to the centre of its travel. For instance, if you intend to change the calibration via software. However, if the meter is to measure 'real' volts, ampères and ohms, P1 has to be set more accurately. All you need for this purpose are a stable voltage of (nearly) 3.999 V, and an accurate voltmeter (min. 3¾ digit, and having an accuracy better than that of the DMM). Connect the test voltage to the DMM inputs, and set the meter to the 4-V range (i.e., autoranging function switched off). To prevent overflow, the input voltage has to stay just under 4 V. The adjustment of P1 is simple: turn the wiper until the DMM reads the same value as the voltmeter you have connected in parallel. That is all! All other ranges are then automatically calibrated.

Next month's instalment will discuss the Fuzzy Control One software in greater detail, along with an example of a fuzzy logic control system that makes use of the multimeter described here.

Reference:
1. Fuzzy logic: an introduction. *Elektor Electronics* July/August 1992.

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LabWindows a is registered trademark of National Instruments.

* names of menus and menu options mentioned in this article may be different from the actual names used in the program.

MICROCONTROLLER-DRIVEN NiCd BATTERY CHARGER

This nickel-cadmium (NiCd) battery charger is capable of charging up to eight cells individually. The power semiconductors needed to accomplish this are all fitted on to a single, large, heatsink, to which the printed circuit board is also secured. That saves 84 wires.

Design by A. Rietjens

THERE are many methods of charging a nickel-cadmium battery. The method used by the present circuit is probably the best: first, discharge the battery, then charge it for a certain period, and, finally, trickle-charge it.

Although there are more chargers that operate on this basis, you will rarely find one that offers continuous adjustment, over a wide range, of the battery capacity and the average charging current. That is a feature uniquely offered by the present charger, which enables you to charge a wide variety of batteries. It must be noted, however, that the batteries which are charged at the same time must have the same nominal capacity. Remarkably, the set charge current is achieved by applying short pulses at the maximum charging current. This ensures good efficiency of the charging process, while the combination with the discharging periods helps to counteract the so-called memory effect. In addition to controlling the charging process, the charger also has a monitoring function. The charging of a battery is stopped the moment the cell voltage rises to a too high value.

8 + 1 = 8

The block diagram of the microcontroller-driven NiCd battery charger is given in **Fig. 1**. The unit consists, broadly speaking, of eight charging circuits and a microcontroller. Each charging circuit (which is divided into a charging and a discharging circuit) handles one NiCd cell (1.2-V battery). The controller is capable of detecting whether a battery is connected or not. If so, it checks the condition of that battery via analogue inputs BT1-BT8 and an on-chip A-D converter. If a battery is detected that needs to be discharged first, the discharging function of the relevant circuit is enabled with the aid of outputs S1-S8. Any time a battery is sufficiently discharged, the associated charging circuit is switched off. When all batteries connected are discharged, the charging circuits are selected and switched to charging.

The desired charging current and the battery capacity are adjusted beforehand by two potentiometers. Like the battery voltage, the setting of these potentiometers is measured by the A-D converter on board the microcontroller. The reset button on the unit is used to signal that a set of batteries has been installed, and that the charging process must begin again.

Four LEDs indicate what the charger is doing. After a reset, the controller starts by checking all eight battery connections. In fact, it checks if a battery is present. If so, the next check is the level of discharging. During this check, the 'CHECK' LED is on. If there are batteries that need to be discharged, this is indicated by the 'DISCHARGE' LED. Another LED, marked
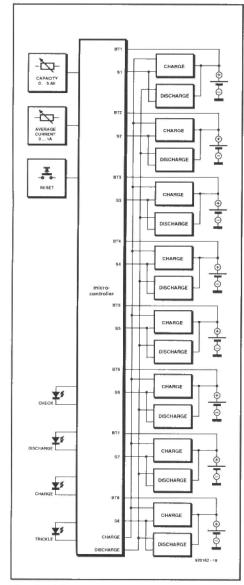
Fig. 1. Block schematic of the microcontroller-driven NiCd charger.

MAIN SPECIFICATIONS

- Charges up to eight NiCd batteries (1.2 V) simultaneously.
- If necessary, batteries are individually discharged.
- Individual monitoring of battery voltage.
- Adjustable charging current: 0-200 mA, 0-1 A, or
                                  0-100 mA, 0-500 mA
- Adjustable capacity: 0-10 Ah or 0-5 Ah, or
                          0-2.5 Ah
- Trickle charging at ¹⁄₂₀th of nominal charging current
- Charging current indicator (LED) for each battery
- Charger state indication using 4 LEDs
- Microcontroller driven
- No adjustments

'CHARGE' lights when all batteries are charged. The 'TRICKLE' LED, finally, lights to indicate that the batteries are kept 'topped up' by a trickle-charging current.

Charging/discharging current and battery voltage

Neither the charging nor the discharging current flows continuously through the battery. This is because the current sources are set to fixed values. The only way of making the (average) current adjustable is, therefore, to give current pulses with an adjustable pulse duration. To generate these pulses, the microcontroller places an appropriate pulse on the 'charge' or 'discharge' control line.

Making the charging current adjustable is not the only reason to opt for current pulses: the pauses between the pulses allow the microcontroller to measure the battery voltage. This can be done without losses introduced by

wires and contacts, since, theoretically, no current flows during the measurement. One complete cycle (current pulse followed by a pause during which the battery voltage is measured) lasts about 2.5 seconds.

The different steps into which the test procedure may be divided are shown in the flow diagram, **Fig. 2**. Each time the procedure is called, the voltage on all battery stations (whether 'occupied' or not) is measured. The variable 'BATCOUNT' indicates the number of the battery station (connection) whose voltage is measured. The state of each output is recorded with the aid of five variables. Three voltage ranges are set up to determine what is connected to the battery terminals. If the voltage is between 0.5 V and 1.8 V, the controller assumes that a battery is connected. If the voltage is between 0.5 V and 1 V, the battery is assumed 'flat'. Finally, if the voltage is greater than 1.6 V, it is assumed to be too high.

The results are evaluated after these three measurements. From a point of view of logic, this part of the flow diagram is not complete. Not shown are the small differences in the charging level assessment, which depend on the state of the charger (check; discharge; charge or trickle). For instance, while in 'charge' mode, it is not necessary to check if the batteries are discharged, since that has already been done. Once the state of a battery at one of the terminals has been measured, the software continues with the next one, until all have been checked. Only then does the next charging cycle begin, taking into account the result of the test routines for each individual battery.

16 current sources and one microcontroller

Before discussing the complete circuit diagram, we first examine the operation of one charging/discharging circuit — see **Fig. 3**. Transistors T25 and

T28 are common to all eight charging/discharging circuits, and serve to switch between these two functions. Each circuit is individually switched on and off by the 'select' line. The bat-
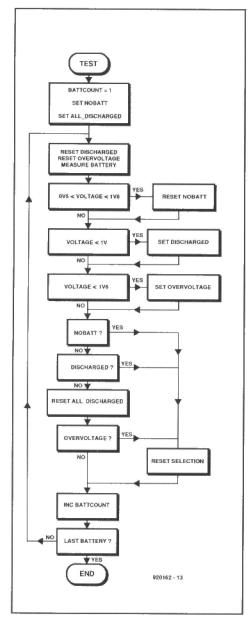
Fig. 2. The state of each battery is continuously checked during the entire charging operation.
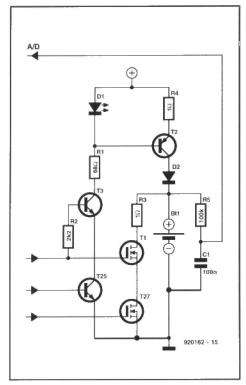
Fig. 3. Basic charging/discharging circuit. The unit has eight of these.

Table 1. Range selections

| | | | R4;R9;R14;R19;R24;R29;R34;R39 | |
			1 Ω	2 Ω
Capacity	P1	JP1 open	0-5 Ah	0-2.5 Ah
Capacity	P1	JP1 closed	0-10 Ah	0-5 Ah
Charging current	P2	S1 closed	0-1 A	0-500 mA
Charging current	P2	S1 open	0-200 mA	0-100 mA

tery voltage is measured by the microcontroller via filter R5-C1. To discharge the battery, the 'select' and 'discharge' lines have to be high simultaneously. The discharging current then flows via resistor R3 (which limits the current to about 1 A), and MOSFETs T1 and T27.

If the 'select' and 'charge' lines are high, current source D1-T2-R4 is switched on, and current is supplied to the battery. LED D1 has two functions. Firstly, the voltage across it is the reference for current source T2. Secondly, it serves as a 'charge' indicator because it flashes when the relevant battery is being charged. D1 is a red LED, which has a typical voltage drop of 1.6 V. After subtracting the base-emitter voltage of T2, this leaves 1 V across R4, so that a current of 1 A flows. This constant current leaves the circuit via the collector of T2, and is fed to the battery. Diode D2 protects T2 against excessive voltages. Since D1 is used as a reference, it **must** be a red LED (the voltage across LEDs depends on the colour). Also, do not use a high-efficiency type in position D1, since that, too, causes an incorrect reference voltage.

As already mentioned, the battery is charged with a current pulse every 2.5 seconds, which is indicated by the LED flashing at the same rate. If the LED does not flash, or flashes irregularly, there is probably something wrong with the relevant battery. Do note confuse irregular flashing with 'slow' flashing (every 50 s), which indicates trickle charging.

The full circuit diagram of the mi-

crocontroller-driven NiCd charger is given in **Fig. 4**. Controller IC1 is a member from the ST62xx family which was introduced in Ref. 1. The eight charging circuit are divided into two groups of four, which are separately powered. In this way, the maximum load on the charging/discharging circuits is limited to 4 A, which is easier to handle than the 8 A which would be required if all circuits were connected to a single supply.

The division into two groups is also found back with T27. To prevent all discharge currents flowing through this transistor, it is shunted by a second power MOSFET, T26. Each of these transistors handles one group of charging/discharging circuits, and, thus, half the total discharging current. Furthermore, the division into two groups comes in handy for the design of the printed circuit board, because it allows the tracks that carry the total charging/discharging current to be kept as short as possible. Transistor T25 does not need 'assistance' since it can easily handle the current drawn by the eight LEDs in the charging circuits on its own.

Since microcontroller IC1 has a limited number of inputs and outputs, the

four modes of the charger (check; discharge; charge; and trickle) are conveyed to the circuit via two outputs only. These two control bits are decoded by demultiplexers IC2a and IC2b. The latter controls LEDs D19 (check), D20 (discharge), D21 (charge) and D22 (trickle). These LEDs indicate the state of the charger. IC2b decodes the two output bits to control T25, T26 and T27. In 'check' mode, these three transistors are switched off, allowing the microcontroller to measure the battery voltage (remember, no current flows at this stage). In 'discharge' mode, T26 and T27 are switched on, while T25 is switched on in 'charge' as well as in 'trickle' mode. Current pulsing is achieved by switching between 'check' mode on the one hand, and 'discharge', 'charge' or 'trickle', on the other.

The charger is adjusted with the aid of P1 and P2 (for the ranges, see Table 1). P1 enables the battery capacity, or, more properly, the energy (in Ah) put into the battery, to be set. This means that the battery charger does not compensate the efficiency of the charging process. Fortunately, that is not a problem because the efficiency of the charging process is relatively high
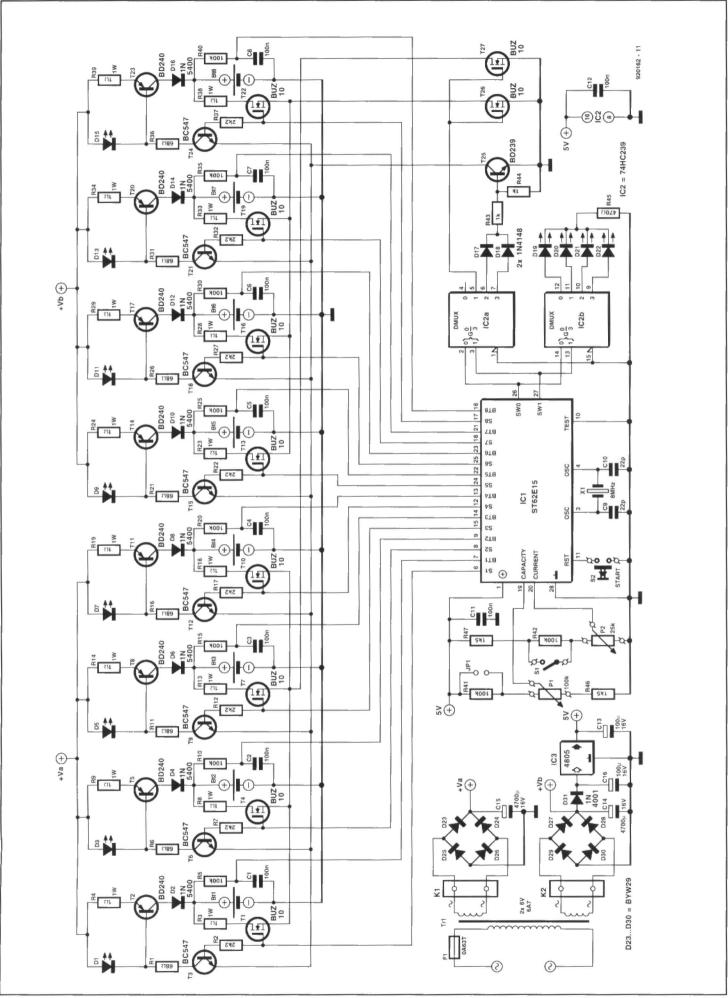
Fig. 4. Circuit diagram of the NiCd charger. Most discrete electronics is contained in the charging/discharging circuits. Inside IC1 lurks a complete computer system with RAM, ROM and an A-D converter.
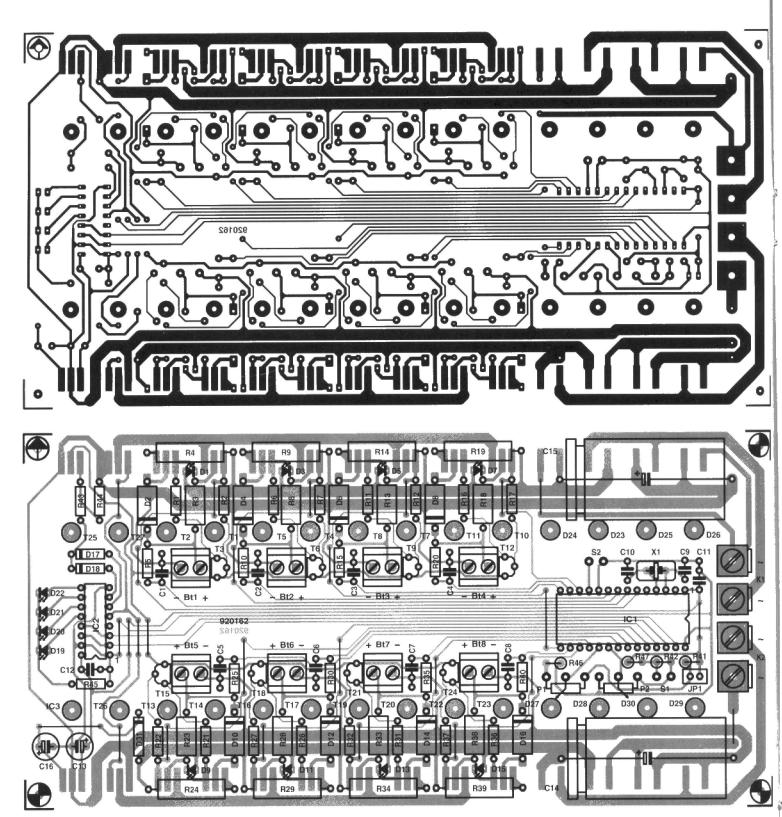
Fig. 5. The printed circuit board is designed to fit on the SK47/100/SA heatsink. Use a photocopy of the component mounting plan as a templatye to drill the holes for the power semiconductors.

by virtue of the high charging current. In practice, you will come very close to a 'full' battery if you set its nominal capacity with P1. If, after having used the batteries, they appear not to have had the full capacity, try setting a higher capacity with P1 next time (however, do not go higher than 1.4 times the nominal capacity).

The second control, P2, allows the average charging current to be set.

That may appear strange, since the current sources pump fixed 1-A pulses through the battery, no matter how small this is. However, by matching the average current to the specification of the battery, this is given sufficient time to recover from the current pulse. Current pulses cause gas bubbles in the battery. Although these disappear as a result of the chemical reaction set off the charging current, this takes

some time. Since the gas bubbles increase the pressure inside the battery, the amount of gas must be restricted. Here, this is achieved by a pause following each current pulse.

If you frequently use small batteries which seem to have problems with the 1-A charging current, it is recommended to change R4 (and its counterparts in the other current sources) from 1 Ω into 2 Ω. This modification

COMPONENTS LIST

Resistors:

8	68Ω	R1;R6;R11; R16;R21;R26; R31;R36
8	2kΩ2	R2;R7;R12; R17;R22;R27; R32;R37
16	1Ω 1W	R3;R4;R8;R9; R13;R14;R18; R19;R23;R24; R28;R29;R33; R34;R38;R39
10	100kΩ	R5;R10;R15; R20;R25;R30; R35;R40;R41; R42
2	1kΩ	R43;R44
1	470Ω	R45
2	1kΩ5	R46;R47
1	100kΩ linear potentiometer	P1
1	25kΩ linear potentiometer	P2

Capacitors:

10	100nF	C1-C8;C11;C12
2	22pF	C9;C10
2	4700µF 16V	C14;C15
2	100µF 16V radial	C13;C16

Semiconductors:

10	LED, red, 3mm	D1;D3;D5;D7; D9;D11;D13; D15;D19;D21
8	1N5400	D2;D4;D6;D8; D10;D12;D14; D16
2	1N4148	D17;D18
1	LED, yellow, 3mm	D20
1	LED, green, 3mm	D22

8	BYW29	D23-D30
1	1N4001	D31
10	BUZ10	T1;T4;T7;T10; T13;T16;T19; T22;T26;T27
8	BD240	T2;T5;T8;T11; T14;T17;T20; T23
8	BC547B	T3;T6;T9;T12; T15;T18;T21; T24
1	BD239	T25
1	ST62E15 microcontroller; supplied ready-programmed; order code: 7071* (see page 70)	IC1
1	74HC239	IC2
1	4805	IC3

Miscellaneous:

8	2-way PCB terminal block, pitch 5mm	Bt1-Bt8
1	fuse 630mA, slow	F1
1	jumper	JP1
4	PCB mount spade terminal	K1;K2
1	SPST switch	S1
1	Press-key	S2
1	Mains transformer 2x6V/6-7A	Tr1
1	8MHz quartz crystal	X1
1	Mains socket with integral fuseholder and switch	
1	Heat-sink SK47/100/SA (Fischer); size: 200x100x40mm	
1	Printed circuit board plus IC1; set order code 920162.	

* part of set 920162.

results in current pulses of 500 mA instead of 1 A (see also Table 1).

Since the energy to be put into the battery is set with the aid of P1, the charging time of the battery is easily computed by dividing the set capacity by the set current. Only if the charging current is at or near the maximum, you will have to allow for some extra time, which goes on account of the microcontroller running state checks on the batteries.

Last but not least, the power supply of the NiCd charger. The mains transformer is a fairly heavy type with two separate 6-V secondary windings, each rated at 6-7 A. Here, too, the supply is divided into two parts to keep the maximum currents within reason. None the less, the rectifier diodes have a pretty hard time, and to keep them cool they have to be fitted on the heatsink, together with the power transistors. That is also why TO-220 style diodes are used. For the rest, the power supply is straightforward: bridge rectifier, smoothing capacitor and a 5-V regulator, IC3, to supply IC1

and IC2. A low-drop voltage regulator is used because of the relatively low transformer secondary voltage (which is necessary to keep the dissipation in the current sources within limits).

Construction

The artwork for the printed circuit board is shown in **Fig. 5**. The PCB is designed so that it forms a sandwich construction with the heat-sink. The power semiconductors are fitted between the board and the heat-sink. First, however, mount all components shown on the PCB overlay (which excludes the TO-220 style power transistors and diodes). It Is best to start with the 26 wire links on the board. Use fairly thick wire for the links next to K2 and at the head of C15, since these wires carry the full supply current. At the track side of the board, fit a 10-kΩ resistor between pin 1 (+5 V) and pin 5 (NMI) of IC1. Although this pull-up resistor should not be required, some of our prototypes of the charger did not work properly without it. Finally,

check the populated PCB for errors, since these are not so easy to correct later.

To enable the sandwich construction to be made, the heat-sink has to be drilled and tapped first. Punch holes into the heatsink, using a photocopy of the component overlay to find the locations (check that your photocopier produces a copy of exactly 100%). All in all, there are 32 holes: four fixing holes, and 28 for the power transistors, diodes and IC3. Drill 2.5mm dia, 15 mm deep, holes. Deburr the holes, because the components have to rest flat on the heat-sink for optimum heat transfer. Next, thread the holes with an M3 tap. The depth of the threading is about 10 mm.

Figure 6 shows the position of the power components between the heat-sink and the PCB. Start by bending the component terminals into the shape shown. Next, mount each component on to the heat-sink, using a 10-mm bolt, insulating material and heat transfer paste. Make sure that each component is fitted the right way around, and at the right location. Next, run a check on short-circuits between the metal tabs and the heat-sink. Place the PCB over the components, so that the terminals rest against the respective copper spots. If necessary, align the components, and tighten the bolts (which are accessible through holes in the PCB). Next, solder the terminals from the side.

Connect the mains transformer, and apply power. LED D19 should light immediately. For a further check on the circuit, you need a nearly exhausted battery. Set the nominal capacity of this battery with P1, and an appropriate charging current with P2. Connect the battery to one of the PCB terminal blocks. On starting the charger by pressing S2, the CHECK LED (D19) should light briefly, followed by the DISCHARGE LED (D20) — provided, of course, that the battery is not completely discharged. If the battery is 'flat', the 'CHARGE' LED lights, and also the LED in the charging circuit to which the battery is connected. Next, all you can do is wait and see if the charger keeps to the charging time that belongs with the setting (capacity/charging current) made with P1 and P2. Since there are no adjustment points in the circuit, it is best to leave it working for a while.

Once the unit works properly, it may be finished mechanically. Great attention should be given to safety precautions for all wires and terminals that carry the mains voltage. In this respect, it is best to use a mains socket with a built-in switch and fuseholder. Note that the switch is not drawn in the circuit diagram, although
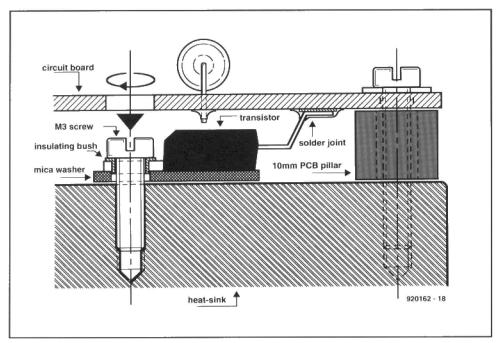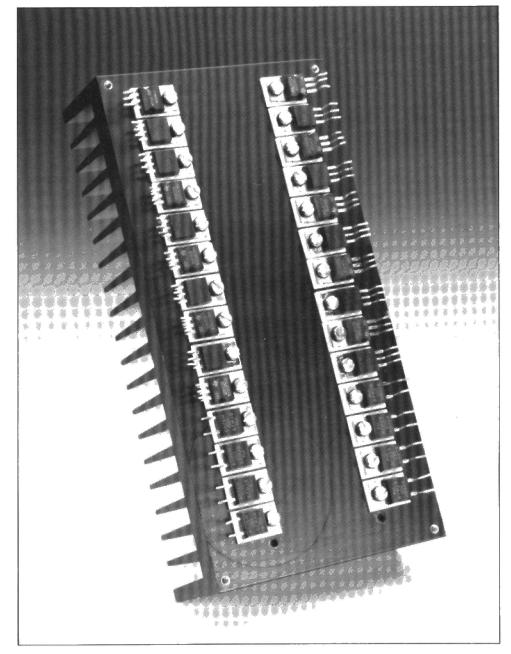
Fig. 6. Illustrating the 'sandwich' construction, with the power semiconductors fitted between the PCB and the heat-sink.

it is essential. The fuseholder holds fuse F1.

The biggest problem in the finishing of the unit is probably the battery holder. Although holders are available for single cells, these are usually suitable for internal or recessed mounting only. In any case, a multi-battery holder as seen in commercially available chargers proved impossible to find as a separate part from electronics retailers. It may, therefore, be a good idea to salvage such a holder from an inexpensive ('no-good-anyway') battery charger. Alternatively, join a couple of single-cell holders, and connect them to the charger via a short cable fitted with a plug. Another alternative, although quite costly, is to use Varta's stackable battery holders (Types RSH4 for 'mono' cells; RSH1,8 for 'baby' cells; and 501RS for 'penlights'). Whatever solution is found to solve the battery holder problem, be sure to keep the wire connections as short as possible, since the ability of the current sources to compensate losses caused by junction resistances.

Finally, scales are readily made for the two potentiometers, since their ranges are linear.

Operation

In general, use the nominal capacity of the battery to set the capacity on the NiCd charger. In virtually all cases, that is sufficient to fully charge the battery. The same goes, basically, for the charging current, which is set in accordance with the battery manufacturer's recommendations. Remember, however, that low temperatures forbid high charging currents. The charging current is too high if the battery temperature runs up to 40 °C at room temperature.

Since the capacity and charging current settings are common to all batteries connected, only batteries with equal nominal capacities can be charged at the same time. If you happen to have a number of batteries with different conditions (charging levels), remember that the charger does not start charging until the last battery is discharged. So, if you are in a hurry, it may be more economical to first charge the most discharged batteries. ∎

References:
1. Maxi micro clock. *Elektor Electronics* July/August 1993.

APPLICATION NOTE

MICRO LINEAR 2035 & 2036
PROGRAMMABLE SINE WAVE GENERATORS

The ML2035 and ML2036 are monolithic sine wave generators that are programmable from d.c. to 25 kHz and from d.c. to 50 kHz respectively. The frequency can be set in steps of 0.5 Hz. They are intended primarily for telecommunications and modem applications that need low-cost and accurate generation of precise test tones, call progress tones, and signalling tones.

The frequency of the sine wave output is derived either from an external crystal or clock input, thus providing a stable and accurate frequency reference. The frequency is programmed by a 16-bit serial data word.

The ML2035 is housed in an 8-pin d.i.p. and the ML2036 in a 14-bit d.i.p. or a 16-pin SO (small outline) case.

Figure 1 shows the block diagrams of the two devices. Both contain a 16-bit shift register and associated 16-bit data latch. The content of the register determines the output frequency via a phase accumulator and 512 point sine look-up table, which will be reverted to shortly. An 8-bit digital-to-analogue (D/A) converter transforms the output of the phase accumulator into an analogue voltage that is smoothed by a filter. Furthermore, both devices have the facility

for a power-down mode, which allows the digital section to be switched off. To that end, the shift register must be loaded with zeros and the LATI input connected to +5 V. The ML2036 has the further facility of an INH(ibit) function, which switches off the output when the next zero crossing of the sine wave is reached.

Whereas the ML2035 has a fixed output level of ±2.5 V_{pp}, that of the ML2036 can be preset by the combination of the reference voltage and the logic state at the GAIN terminal. If, for instance, the GAIN pin is at +5 V (logic high), the peak output voltage is equal to the reference voltage ($V_{o(pp)} = 2V_{ref}$). If the GAIN pin is at 0 V (logic low), the peak output voltage is equal to $V_{ref} / 2$, so that $V_{o(pp)} = V_{ref}$.

The ML2036 also has two additional clock outputs, fCLKIN / 2 and fCLKIN / 8, a power-down input and isolated grounds for its analogue and digital sections.

The power requirement for both chips is ±5 V; the negative voltage is needed for the analogue section.

The digital inputs of both devices are TTL/CMOS compatible.

Waveforms

Figure 2 illustrates how the devices generate the sine waves. A complete sine wave is resolved into 2^{21} phases. The 16-bit data register decides how many of these fractions will be enclosed by two successive clocks (**Fig. 3**). In this way, low values in the 16-bit register produce low frequencies since many of the phases are scanned. High 16-bit values result in high frequencies since many phases are 'ignored'.

The adder and the latch form the phase accumulator that contains the actual phase status. The accumulator is clocked at $f_{CLKIN}/4$. The value stored in the data latch is added to the phase accumulator every 4 cycles of CLKIN. The frequency of the analogue output is equal to the rate at which the accumulator overflows and is given by:

$$f_0 = [f_{CLKIN} \times (D_{15} - D_0)_{DEC}] / 2^{23}.$$

Thus, the length of each phase caused by a change of 1 in the content of the register is given by:

$$\Delta f = f_{CLKIN} / 2^{23}.$$
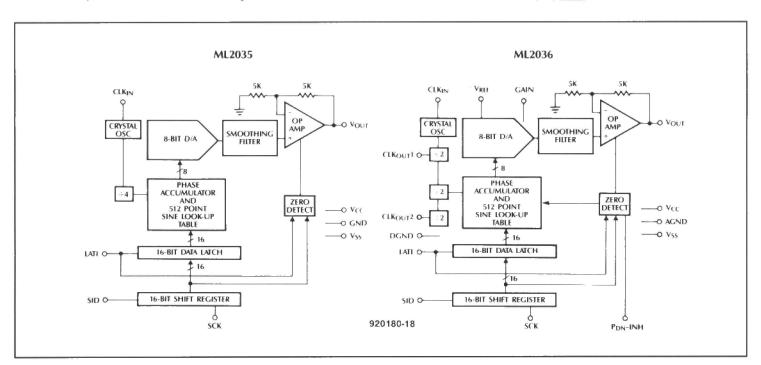
Fig. 1. Block diagrams and pinouts of sine wave generators ML0235 and ML0236.

Fig. 2. The functional diagram applies to both devices.
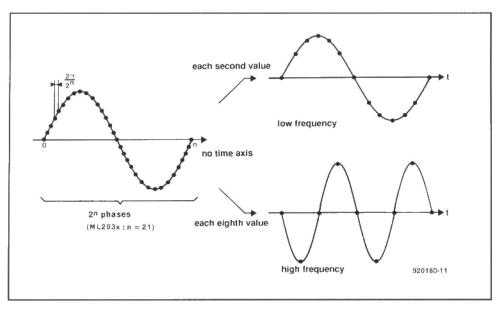
For instance, if the crystal frequency, f_c, is equal to the clock, f_{CLKIN} of 4.194304 MHz,

$$\Delta f = 0.5 \text{ Hz},$$
and
$$f_{o(max)} = f_{CLKIN} \times 2^{16}/2^{21} = 32.768 \text{ kHz}.$$

Only the eight highest valued of the 21 bits are processed further; the highest valued bit is the polarity symbol.

Apart from symmetry around the time axis, a sine wave also has symmetry with respect to the peak values of the waveform (**Fig. 4**). This property is used here. With the aid of the second highest bit, the quadrant complementor translates the 7-bit phase value in a manner that a sine look up table with values for 128 phase steps between 0 and $\pi/2$ suffices to compute the output amplitude. The next step in the process is the reemployment of the polarity symbol to ascertain whether a positive or negative half wave must be output (sign complementor). After a second output latch follow the D-A converter and the low-pass filter.

Owing to the phase quantization nature of the frequency generator spurious tones can be present in the output in the range of −55 dB relative to the fundamental. The energy from these tones is included in the signal-to-noise+distortion specification. The frequency of these tones can be very close to the fundamental and it is, therefore, not practical to filter them out.

The sine wave generator comprises a sine look-up table, a DAC, and an output smoothing filter. The sine look-up table is addressed by the phase accumulator. The DAC is driven by the output of the look-up table and generates a staircase representation of a sine wave.

The filter smooths the analogue output by removing the high frequency sampling components. The resultant voltage on V_{OUT} is a sinusoid with all distortion components at least 45 dB below the fundamental.

The ML2035 provides a peak sinusoidal voltage of $\pm V_{CC}/2$. The ML2036 has a V_{REF} input that can be tied to V_{CC} or generated from an external voltage. With the GAIN input equal to a logic 1, the sine wave peak voltage is equal to $\pm V_{REF}$; with the GAIN input equal to a logic 0, the peak voltage is $\pm V_{REF}/2$. The sine wave output is referred to AGND for the

Fig. 3. Sinusoidal signals can be generated from preset digital values.
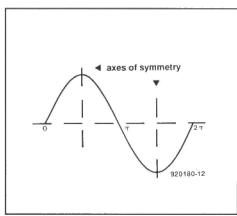
Fig. 4. A sinusoidal signal is symmetrical not only around the time axis, but also with respect to its peak values.
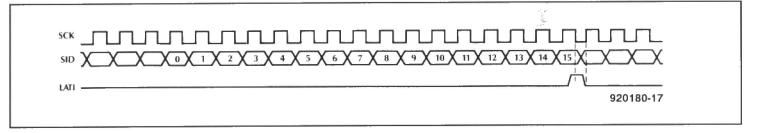
Fig. 5. Serial interface timing.

ML2036 and GND for the ML2035.

Although the analogue section is designed to operate over a range from d.c. to 50 kHz, owing to slew rate limitations, the peak-to-peak output voltage must be limited to $V_{OUT(pp)} \leq (125 \text{ kV} \times \text{Hz}) / f_{OUT}$. For example, on the ML2036 an output of 50 kHz must be limited to 2.5 V_{pp}. Since the ML2035 peak-to-peak output voltage is equal to V_{CC}, the maximum output frequency must be limited to 25 kHz for $V_{CC} = 5$ V. V_{OUT} can drive 1 kΩ, 100 pF loads and swing to within 1.5 V of V_{CC} and V_{SS}, provided the slew rate limitations mentioned above are not exceeded.

The output offset voltage, V_{OS}, is a function of the peak-to-peak output voltage and is specified as 25 mV + ($\pm 10 \times V_{OUT(pp)}$) max. For example, if $V_{OUT(pp)} = 2.5$ V, $V_{OS} = 50$ mV max.

The crystal oscillator generates an accurate reference clock for the programmable frequency generator.

The internal clock can be generated with a crystal or an external clock.

If a crystal is used, it must be placed between CLK_{IN} and DGND of the ML2036 or GND of the ML2035. An on-chip oscillator will then generate the internal clock. No other external components are required. The crystal should be a parallel resonant type with a frequency between 3 MHz and 12.4 MHz. It should be placed physically as close as possible to the $CLK_{IN}$ and DGND (or GND). Its maximum equivalent series resistance should be 15 Ω at drive levels of 1–200 μW, or 30 Ω at drive levels of 10 nW to 1 μW. A typical

load capacitance is 18 pF. The maximum case capacitance is 7 pF.

The ML2036 has two clock outputs that can be used to drive other external devices. The $CLK_{OUT}1$ output is a buffered output from the oscillator divided by 2. The $CLK_{OUT}2$ output is a buffered output from the oscillator divided by 8.

The digital interface consists of a shift register and data latch. The serial 16-bit word on SID is clocked into a 16-bit shift register on leading edges of the serial shift clock, SCK. The LSB should be shifted in first and the MSB last as shown in **Fig. 5**. The data that has been shifted into the shift register is loaded into a 16-bit data latch on the trailing edge of LATI. To ensure that true data is loaded into the data latch from the shift register, LATI trailing edge should occur when SCK is low as shown in **Fig. 1**. LATI should be low while shifting data into the shift register to avoid inadvertently entering the power down mode as described below. Note that all data is entered and latched on edges, not levels, of SCK and LATI.

The power down mode of the ML2035 can be selected by entering all zeros into the shift register and applying a logic 1 to LATI. A zero data detect circuit detects when all bits in the shift register are zeros. In this state, the power consumption is reduced to about 11.5 mW, and V_{OUT} goes to 0 V. The master clock, CLK_{IN}, can be left active or removed during the power down mode.

The ML2036 has an inhibit mode and a power down which are controlled by the

three-level P_{DN}-INH input. When a logic 1, V_{13}, is applied to the P_{DN}-INH pin, the power down mode is entered in the same way as described for the ML2035. Also, the ML2036 will be placed in the power down mode by applying a logic 0 to the P_{DN}-INH pin.

If V_{SS} to $V_{SS} + 5$ V, V_{12}, is applied to the P_{DN}-INH pin, the inhibit mode is entered by shifting all zeros into the shift register and applying a logic 1 to the LATI pin. Once the inhibit mode is entered, V_{OUT} will complete the last half cycle of the sine wave and then be held at about V_{OS}, such that no voltage step occurs.

The analogue circuits in the device are powered from ±5 V (V_{CC} to V_{SS}) and are referred to AGND.
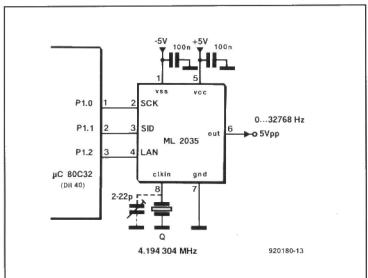
The digital circuits in the device are powered from 0–5 V (V_{CC} to DGND).

For the ML2036, it is recommended that AGND and DGND be connected together close to the device and have a good connection back to the power source.

It is recommended that the power supplies to the device be bypassed by placing decoupling capacitors from V_{CC} to AGND (GND for the ML2035) and V_{SS} to AGND (GND for ML2035) as physically close to the device as possible.

Interfacing

The timing of the serial data input (SID), serial clock (SCK) and the latch input (LATI) is shown in **Fig. 5**. The leading edge of the clock pulses determines the exact instant at which the data are transferred from the SID to the shift register, starting with the LSB and
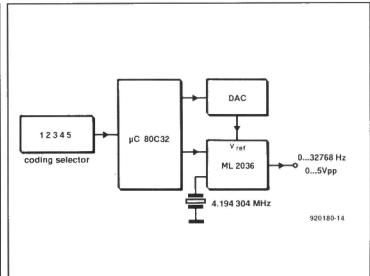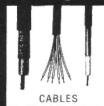
Fig. 6. Application of ML2035.
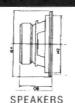
Fig. 7. Block diagram of an ML2036 application.

ending with the MSB. During the clocking in, the LATI is logic low (0 V), but, as the diagram shows, it goes high during the last data bit. The trailing edge of the LATI pulse enables the transfer of the data in the shift register to the 16-bit latch. This must happen during the logic low phase of the clock to prevent accidental transfer to the power down state.
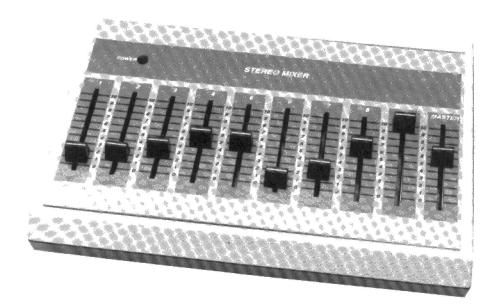
Applications

A practical circuit using the ML 2035 is shown in **Fig. 6**. It is used to set the frequency of an 80C32 microcontroller in steps of 0.5 Hz between d.c. and 32 765.5 Hz. Since the crystal oscillates in parallel resonance, the exact frequency can be set with the trim-mer across the crystal.

The block diagram in **Fig. 7** is an audio frequency generator with variable output level based on an ML 2036. The V_{ref} output of the ML 2036 is linked to a D-A converter which presets the output level.   **END**

STEREO MIXER

Design by Q. Gregory

A block diagram of the mixer is shown in **Fig. 2**. Each input has a matching circuit to ensure that the signal source is not unduly overloaded. The output of each input stage may be adjusted to the required level with a (stereo) potentiometer. The outputs of all input stages are combined in a summing amplifier. This amplifier is provided with a (stereo) potentiometer to enable the output level to be matched to the sensitivity of the unit to which the mixer is connected.

The circuit

The circuit of a single input stage is shown in **Fig. 1a** and that of the summing amplifier in **Fig. 1b**.

Referring to the left-hand channel (the right-hand channel is, of course, identical), the input signal is applied to the inverting (–) input of IC_{1a}. The amplification of this stage is $\alpha = -R_2/R_1 = -1$. The minus sign indicates that the stage is an inverting amplifier. The amplification factor, α, may be altered by giving R_2 (and, of course, R_5) a different value.

High-frequency interference signals are prevented from appearing at the out-

The mixer is of modular design so that the constructor can decide how many inputs should be provided
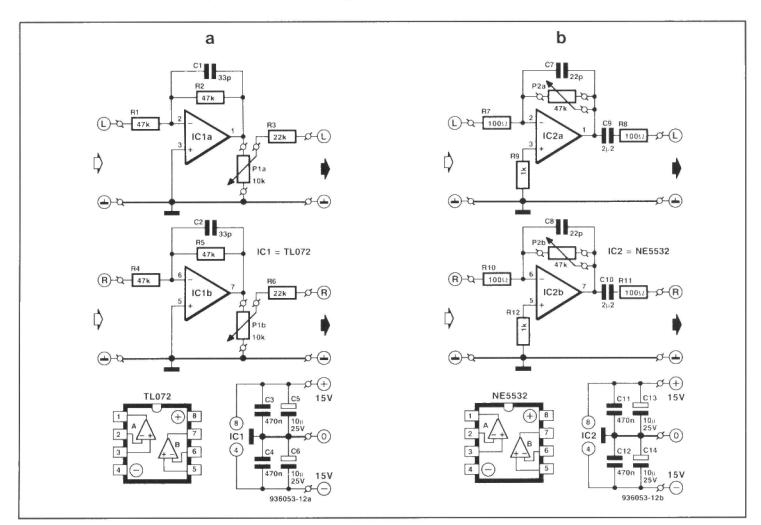
Fig. 1. Circuit diagram of (a) one of the input stages, and (b) the output amplifier.
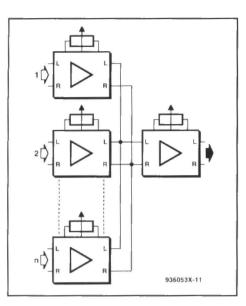
Fig. 2. Block diagram of the stereo mixer.
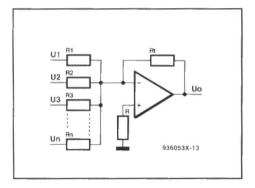
Fig. 3. Simplified representation of the summing circuit.

put (pin 1) by decoupling capacitor C_1. Network R_2-C_1 forms a low-pass filter with a cut-off frequency of around 100 kHz. If the value of R_2 is changed, the cut-off frequency will shift (it is inversely proportional to the change in value of R_2, that is, if R_2 is doubled in value, the cut-off frequency is halved). It is, therefore, advisable not to make R_2 too large, otherwise the cut-off frequency may fall in the audio range (20 Hz to 20 kHz). On the other hand, too low a value of R_2 would shift the cut-off frequency too far upwards.

Circuit IC_2 sums the outputs of all the input stages as shown, simplified, in **Fig. 3**. Its output voltage, U_0, is given by the formula:

$$U_0 = -(U_1 + U_2 + U_3 \ldots + U_n),$$
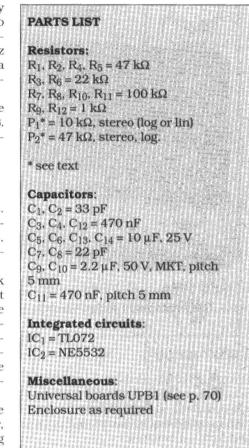
in which n is the number of input stages. This formula applies only if all input resistors, R_1, R_2, ... R_n have the same value. In that case, each of the input stages functions as an inverting ×1 amplifier.

As usual, if the value of the feedback resistor, P_2 in **Fig. 1b**, is greater than that of the input resistor, the gain rises above unity. In the present design, the input resistance $(R_3 + R_7) \approx 22\ k\Omega$, so that the amplification $(P_2 / (R_3 + R_7)$ can be varied between 0 and ×2. As in the input stages, the feedback resistor is decoupled by a capacitor (C_7).

The output of the mixer is available after a series RC network. The capacitor, C_9, prevents any direct voltage appearing at the output. The resistor, R_8, obviates any

tendency to oscillation caused by a capacitive load (such as long screened cables).

The mixer is powered by a regulated ±15V supply that can provide a current of not less than 100 mA.
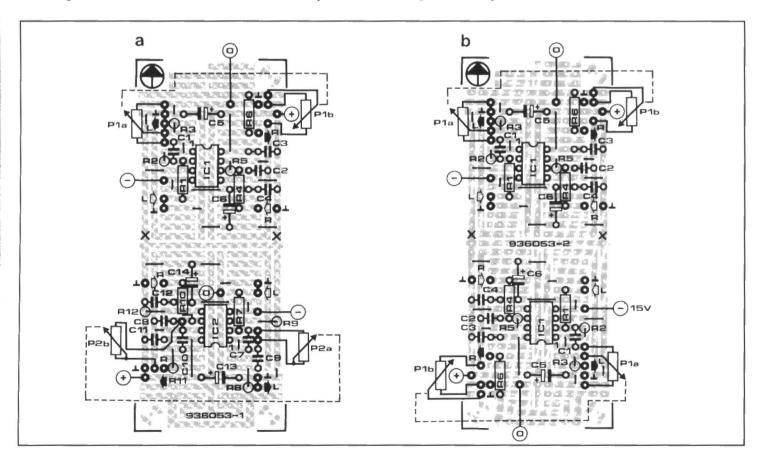
Fig. 4. Construction is best done on a number of universal boards No. UPB1 (see p. 70). At the left, a combination of one stereo input stage and the output stage on one board; at the right, two input stages on another board.
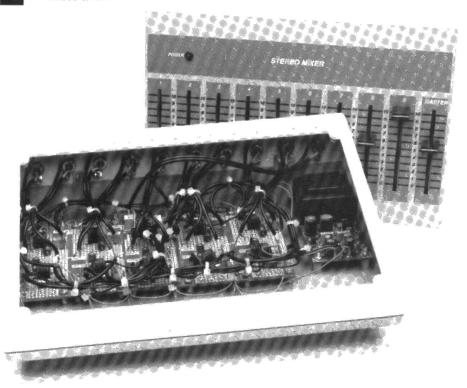
Fig. 5. This photograph shows the large number of screened cables required.

Construction

The prototype has nine stereo input channels, but as already stated, this number is up to individual requirements. If monaural inputs are required, replace P₁ by two mono potentiometers.

The prototype has 10 slide potentiometers

(one for the output stage). One input stage and the summing amplifier can be built on a universal board (UPB 1) as shown in **Fig. 4**. Further input stages can be built, in pairs, on the same type of board. The prototype thus uses five of these boards.

Start by laying the wire bridges. Use sock-

ets for the ICs so that these can be replaced easily if and when required. Use PCB pins for all external connections because, as will be seen during the construction, these are indispensable at a later stage.

When all boards and the power supply have been constructed, they can be assembled in a suitable enclosure (the best is one with a slanting front panel specially designed for mixers).

The use of slide potentiometers is strongly recommended, because these show at a glance the setting of each channel. This type of control is dearer than a rotary control and it also has the disadvantage of requiring a slot rather than just a round hole. Fit the (slide) potentiometers to the front panel on short spacers.

Next, drill the holes in the rear panel for the audio sockets (**Fig. 7**) and fit the sockets with their earth terminal at the top. If a metal enclosure is used, the sockets should be insulated from it to obviate earth loops.

Fit the boards and the power supply in the enclosure. Keep the supply as far away from the inputs as possible to minimize the risk of mains hum. Fit the mains input cable with a strain relief.

All audio connections must be made in screened cable (**Fig. 5**) to minimize any hum pick-up. There are thus four screened cables to the potentiometer in each input stage. The earth terminal of each stereo potentiometer must be connected to the screen of the cable. Interconnect the screens of the left-hand and right-hand channels and solder the joints to the ground terminals
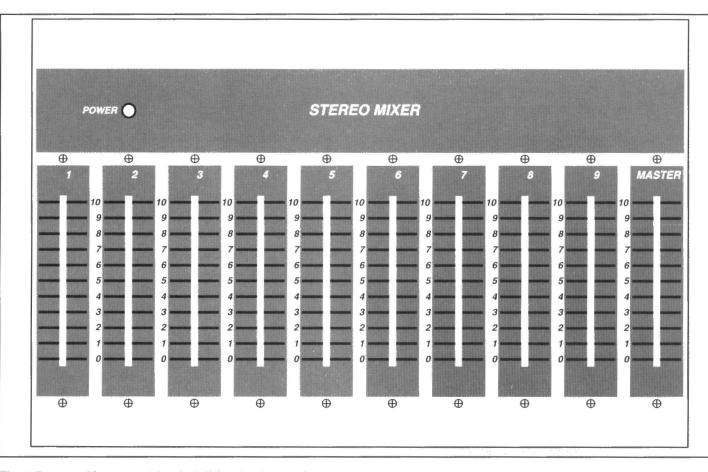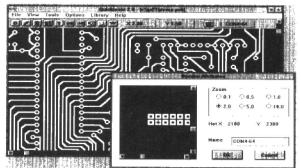
Fig. 5. Proposed front panel (scale 1:1) for the stereo mixer.

on the board.

The potentiometer in the summing amplifier needs to be connected by only two screened cables, because its wiper is linked to one of its other terminals.

The (already good) signal-to-noise ratio may be improved further by the use of metal film resistors instead of carbon types. Also, use conductive-plastic type slide potentiometers instead of carbon types. Furthermore, it may be necessary to fit the power supply in a separate enclosure.

Testing

Connect the mixer to a suitable output amplifier (and speakers) and apply an audio signal to each input in turn. Set the master volume control half-way and check that the volume of input can be adjusted between nil and maximum.

When this is so, check that the volume of the composite signal can be adjusted as required with P_2. If the sound increases too rapidly, it is likely that this potentiometer has been connected the wrong way around (since this control has a logarithmic characteristic, it can be connected correctly in only one way). This error is remedied by connecting the wiper of P_2 to the other terminal and turning the control around (180°).

END

Fig. 7. Recommended way of mounting the audio sockets on the rear panel.

FIGURING IT OUT

PART 9 – REACTIVE NETWORKS

By Owen Bishop

This series is intended to help you with the quantitative aspects of electronic design: predicting currents, voltage, waveforms, and other aspects of the behaviour of circuits. Our aim is to provide more than just a collection of rule-of-thumb formulas. We will explain the underlying electronic theory and, whenever appropriate, render some insights into the mathematics involved.

Last month we used complex numbers for circuit analysis, but reverted to using Pythagoras and inverse tangents for evaluating the final result. What we need to do next is to formalize this process. We represent a given complex number z by a point in the complex number plane, quoting its coordinates (a, b) in the form

$$z = a + \mathbf{j}b. \qquad \text{[Eq.55]}$$

These are rectangular coordinates, and the complex number is said to be expressed in **rectangular form**. Another way of specifying the position of a point in a plane is to give its **polar coordinates**. The relationship between the two kinds of coordinate is shown in **Fig. 77**. In this figure:

$$a = r \cos \theta; \qquad \text{[Eq. 56]}$$
$$b = r \sin \theta. \qquad \text{[Eq. 57]}$$

Substituting in Eq. 55 we find:

$$z = r \cos \theta + \mathbf{j}r \sin \theta,$$
or
$$z = r (\cos \theta + \mathbf{j} \sin \theta). \text{ [Eq. 58]}$$

This is the **polar form** of z. The only essential pieces of information in this formula are the radius r and the angle θ. We adopt a shorter way of writing out the polar form by quoting r and θ, but leaving out the 'cos' and 'jsin', which are taken as understood, all complex numbers having the same format. This leaves us with:

$$z = r \angle\theta, \qquad \text{[Eq. 59]}$$

which means the same thing as Eq. 58, but is much quicker to write and much easier to comprehend. In this expression, we refer to r as the **modulus** and to
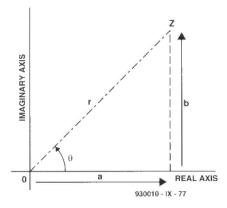
Fig. 77.

θ as the **argument** of the complex number.

Conversions

The two final examples last month showed how to convert from rectangular form to polar form. Given $z = a + \mathbf{j}b$, we calculate:

$$r = (a^2 + b^2)^{1/2}$$
and
$$\theta = \tan^{-1}(b/a),$$

and write the result in the form of Eq. 59. There is a slight problem, which is that there are two possible values of an inverse tan-

gent. These are 180° apart. A simple sketch or inspection of the signs of a and b tells us the quadrant in which z is situated.

Example: convert $z = -4 -\mathbf{j}5$ into polar form. First find
$$r = (4^2 + 5^2)^{1/2} = 6.40.$$
Next, find
$$\tan^{-1}(-5/-4) = 51.34°.$$
But both a and b are negative, so the point must be in the third quadrant. This means that $\theta = 180 + 51.34 = 231.34°$. The result:

$$z = 6.40 \angle 231.24°.$$

Converting from polar form to

rectangular form uses Eq. 56 and 57, the result being written in the form of Eq. 55.

Example: convert $z = 50 \angle 36°$ into rectangular form
$$a = 50 \cos 36° = 40.45;$$
$$b = 50 \sin 36° = 29.39.$$
Result: $z = 40.45 + \mathbf{j}29.39$.

Most scientific calculators have both conversions as built-in programs. Their usefulness depends on the fact that adding and subtracting complex numbers is easier when they are in rectangular form, but multiplying and dividing is easier when they are in polar form. In the course of an analysis we may convert from one form to the other and back again several times, according to which operation is currently required.

The rule for multiplication is: **multiply the moduli, sum the arguments**.

Example: multiply $4 \angle 60°$ by $2 \angle 10°$. Multiply moduli: $4 \times 2 = 8$. Sum the arguments: $60° + 10° = 70°$. Result: $8 \angle 70°$.

Conversely, the rule for division is: **divide the moduli, find the difference between the arguments**. This short, easily remembered form of the rule does not specify which modulus to divide by which, or which argument to subtract from which, but commonsense applies, as in this example: divide $6 \angle 85°$ by $2 \angle 40°$. Divide moduli: $6/2 = 3$. Difference of arguments: $85 - 40 = 45$. Result: $3 \angle 45°$.

Network analysis

Figure 78 shows a reactive network in which we are required to find the voltages and currents for all components. The applied signal has a peak value of 200 V and the frequency is 3183 Hz. We begin by rewriting the capacitance as a complex impedance:

Fig. 78.

$X_C = -j\omega C = -j50.$

Taking node B to be at 0 V, and considering node A at U_A V, by KCL:

$I_1 + I_2 + I_3 = 0,$

or

$$\frac{U_A - 200}{40} + \frac{U_A}{20} + \frac{U_A}{-j50} = 0$$

since $I = U / X$ for each component. This equation is simplified:

$$U_A \left(\frac{3}{40} + \frac{1}{-j50} \right) = 5$$

$$U_A \left(\frac{-j150 + 40}{-j2000} \right) = 5$$

$$U_A = \frac{-j10000}{40 - j150}.$$

Here we have to divide one complex number by another: convert to polar form and divide:

$$U_A = \frac{10000 \angle -90^0}{155.24 \angle 75.07^0}$$

$$= 64.416 \angle -14.93^0.$$

Having found U_A, we know the pd across the 20 Ω resistor and the capacitor, but need to find the pd across the 40 Ω resistor. Since we are, as usual, taking the applied voltage as the reference for phase angle, the polar form of this is $200 \angle 0^\circ$. Calculating U_{40}:

$$U_{40} = 200 \angle 0^\circ - 64.416 \angle -14.93^\circ.$$

Here we have to subtract: convert to rectangular form:

$$U_{40} = (200 + j0) - (62.241 - j16.596)$$
$$= 137.759 + j16.596.$$

Convert the result back to polar form to express it as a phasor:

$$U_{40} = 138.755 \angle 6.869^\circ.$$

Now that we have the pd across all components, we calculate the currents:

$I_1 = (138.755 \angle 6.869^\circ)/40$
$= 3.4689 \angle 6.869^\circ;$
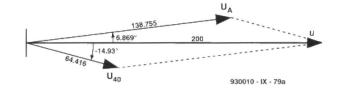
$I_2 = (64.416 \angle -14.93^\circ)/20$
$= 3.2208 \angle -14.93^\circ;$

$I_3 = (64.416 \angle -14.93^\circ)/50 \angle -90^\circ$
$= 1.2883 \angle 75.07^\circ.$

If you try to convert a number such as $-j50$ into polar form with a calculator, you will prob-

ably get an error message. This is because you are asking the calculator to evaluate $\tan^{-1}(-50/0)$. But we know that the '$-j$' means 'turn 90° clockwise', so the conversion may be written out directly as $50 \angle -90°$, as in the equation for I_3.
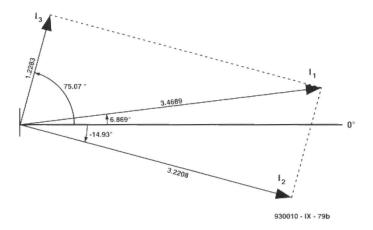
j in determinants

Simultaneous equations that include complex numbers can be solved by determinants with the method explained in Part 4. **Figure 80** is an example of mesh analysis in which we are required to find the value of I_1. The complex impedances are stated beside each component.

As usual, we write an equation for each mesh, including the complex impedances of the capacitor and the inductor:

$$I_1 (8 - j5) - I_2 (8) = 50 + j0;$$

$$-I_1 (8) + I_2 (8 + j4) = 0.$$

The righthand side of the first equation expresses the applied

voltage in rectangular form. This simplifies to just 50.

Following the technique described in Part 4, we write the determinant equation for I_1:

$$I_1 = \frac{\begin{vmatrix} 50 & -8 \\ 0 & 8+j4 \end{vmatrix}}{\begin{vmatrix} 8-j5 & -8 \\ -8 & 8+j4 \end{vmatrix}}.$$

The value of the determinant in the numerator is
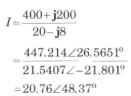
$$50 (8 + j4) - 0 = 400 + j200.$$

The value of the determinant in the denominator is

$(8 - j5)(8 + j4) - 64$
$= 84 - j8 - 64 = 20 - j8.$

Multiplying $(8 - j5)$ by $(8 + j4)$ could be done after converting them to polar form but, with such small coefficients, a straightforward algebraic multiplication is easier. The equation for I_1 simplifies to a quotient:

$$I = \frac{400 + j200}{20 - j8}$$

$$= \frac{447.214 \angle 26.5651^0}{21.5407 \angle -21.801^0}$$

$$= 20.76 \angle 48.37^0.$$

We convert to polar form to evaluate the quotient and state the result in polar form. The peak current in Mesh 1 is 20.76 A, clockwise, leading the applied voltage by 48.37°.

The complex numbers in the determinants of this example are few and simple, but they illustrate the point that determinants may include complex numbers without altering the essential routine of the mesh analysis.

Thevenin equivalent

The complex Thevenin equivalent is calculated in the same way as described in Part 3, but using complex numbers. As an example, we calculate the Thevenin voltage, U_{TH}, and impedance, Z_{TH}, between terminals A and B of the network of **Fig. 81**. In this figure, U_{TH}, defined as the open-circuit voltage, is the voltage across the 4 Ω resistor and the inductor; there is no pd across the 2 Ω resistor, because the circuit between A and B is open. If I is the current circulating in the loop:

$$U_{TH} = I (4 + j3)$$

$$= \frac{10 \angle 0^0}{4 - j2 + j3} \times (4 + j3)$$

$$= 12.127 \angle 22.835^0.$$

The reader may like to verify the intermediate stages of this calculation.

The Thevenin impedance is calculated with the second method from Part 3, in which we replace the voltage source by a short circuit and then apply the technique of network reduction. The network is then equivalent to 4 Ω and $j3$ Ω in series, in parallel with $-j2$ Ω, and this is in series with 2 Ω.

$$Z_{TH} = \frac{(4 + j3)(-j2)}{4 + j3 - j2} + 2$$

$$= \frac{6 - j8}{4 + j} + 2$$

$$= \frac{6 - j8 + 8 + j2}{4 + j}$$

$$= \frac{14 - j6}{4 + j}$$

$$= 3.694 \angle -37.235^0.$$

930010 - IX - 79a

930010 - IX - 79b

Fig. 79.

930010 - IX - 80

Fig. 80
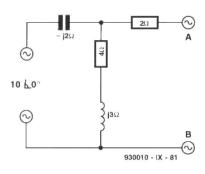
Fig. 81.

Filters

Of all types of circuit, filters are those most concerned with the effects of varying frequency. Consequently, complex numbers are invaluable for analysing filter circuits. We begin with the simplest possible example, a low-pass RC passive filter (**Fig. 82**). Treating this as a potential divider, and assuming that the load current is negligible, we arrive at the ratio

$$U_{out}/U_{in} = X_C/(R + X_C). \quad \text{[Eq. 60]}$$

Writing the capacitor reactance as a complex number:

$$U_{out}/U_{in} = \frac{1/\mathbf{j}\omega C}{R + 1/\mathbf{j}\omega C}$$

Multiplying throughout by $\mathbf{j}\omega C$:

$$U_{out}/U_{in} = 1/(\mathbf{j}\omega RC + 1). \quad \text{[Eq. 61]}$$

For example, given that $\omega = 10^5$ (f = 15,915 Hz), R = 1 kΩ, and C = 10 nF, we find that $\omega RC = 1$. The expression reduces to

$$\begin{aligned} U_{out}/U_{in} &= 1/(\mathbf{j} + 1) \\ &= 1/1.414 \angle 45° \\ &= 0.707 \angle -45°. \end{aligned}$$

The output voltage is reduced to 0.707 of the input voltage and there is a phase lag of 45°. The frequency on which this example is based is the –3 dB point of the filter. Let us see what happens if we double the frequency but keep component values unchanged. Now, $\omega RC = 2$ and:

$$\begin{aligned} U_{out}/U_{in} &= 1/(\mathbf{j}2 + 1) \\ &= 1/2.236 \angle 63.43° \\ &= 0.447 \angle -63.43°. \end{aligned}$$

The output voltage is smaller, showing that this is a low-pass filter, and the phase lag is increased. Note that when the frequency becomes higher, the effect of the '1' in the denominator becomes relatively less. Doubling of frequency approximately halves the output voltage; in other words, output falls at the rate of 6 dB per octave.

This technique is for calculating output and phase lag for any passive RC filter at any frequency. The same principles are applicable to a high-pass filter (with R and C interchanged) or to an LC filter.

The performance of the filter is affected if there is an appreciable load on it. In **Fig. 83**, the load resistor is in parallel with the capacitor. Their parallel impedance is

$$Z_{CL} = X_C/R_L/(X_C + R_L). \quad \text{[Eq. 62]}$$

Substituting Eq. 62 in Eq. 60:

$$U_{out}/U_{in} = Z_{CL}/(R + Z_{CL}).$$
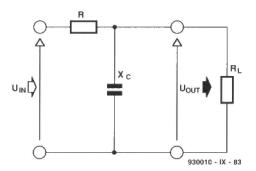
Fig. 83.

Omitting intermediate steps, we arrive at a useful result:

$$U_{out}/U_{in} = 1/(1 + R/R_L + \mathbf{j}wRC). \quad \text{[Eq. 63]}$$

If R_L is infinitely large, this equation reduces to Eq. 61, which is to be expected. As an example, keep other values unaltered and make R_L = 10 kΩ, with $\omega = 10^5$, as in the first filter example:

$$\begin{aligned} U_{out}/U_{in} &= 1/(1 +0.1 + \mathbf{j}) \\ &= 1/(1.1 + \mathbf{j}) \\ &= 1/1.487 \angle 42.27° \\ &= 0.672 \angle -42.27°. \end{aligned}$$

The output voltage and phase lag are both reduced slightly by a 10 kΩ load.

The approach used above may be applied to the analysis of active filters, in which operational amplifiers are employed. The analysis is more involved than that for a passive filter, but the same principles apply and, as far as the topic of complex numbers is concerned, there is nothing new to add.

Fig. 82.

Exponential form

While on the subject of representing complex numbers, the **exponential form** is useful in some applications. The relationship between this and the polar form is:

$$r \angle \theta = re^{\mathbf{j}\theta}.$$

In this equation, θ must be expressed in radians. One advantage of the exponential form is that it makes it possible to take logarithms of complex numbers. Another advantage, more important from the electronic point of view, is that this form is more amenable to the Laplace transformation. This is a topic that we shall deal with in later issue.

TO BE CONTINUED

Test yourself

1. Multiply $(2 + \mathbf{j}3)$ by $(5 - \mathbf{j}4)$ in rectangular form. Then convert them both to polar form and multiply them in this form. Convert the product back to the rectangular form to confirm that the 'multiply/sum' rule is true.
2. Divide $(4 + \mathbf{j}7)$ by $(2 - \mathbf{j}3)$ in rectangular form. Convert to polar form and divide. Convert back to rectangular form to confirm that the 'divide/difference' rule is true.
3. Confirm the correctness of the analysis of **Fig. 76** by converting the currents into rectangular form and checking that $I_1 = I_2 + I_3$.
4. Find the current passing through the resistor in **Fig. 78** (beware inverse tangents).
5. Given a low-pass filter as in **Fig. 81**, but with R = 100 Ω, C = 10 μF and f = 400 Hz, calculate U_{out}/U_{in} and the phase angle. What is the effect of feeding the output to a resistive load of 4 kΩ?

Answers to
Test yourself (Part 8)

1. $9 + \mathbf{j}5$.
2. $10 - \mathbf{j}3$.
3. $1.6 - \mathbf{j}2.6$.
4. $1 + \mathbf{j}8$.
5. $9 + \mathbf{j}37$.
6. $18 - \mathbf{j}4$.
7. $4 - \mathbf{j}5$.
8. $0.466 + \mathbf{j}0.086$.
9. ω = 314.2; X_L = $\mathbf{j}31.42$ Ω; $X_C = -\mathbf{j}67.72$ Ω; $I_R = 0.00833U$; $I_L = -\mathbf{j}0.0318U$; $I_C = \mathbf{j}0.0148U$; $I = 0.0189U$, lagging by 63.9°. Currents in amperes.
10. ω = 942.5; X_L = $\mathbf{j}94.25$ Ω; $X_C = -\mathbf{j}22.59$ Ω; $I_R = 0.00833U$; $I_L = -\mathbf{j}0.0106U$; $I_C = \mathbf{j}0.0443U$; $I = 0.0337U$, leading by 76.1°. When t = 2 s, U = 88.8 mV, I = 2.99 mA.

AUTORANGING FREQUENCY READOUT

The frequency meter described here has a maximum input frequency of about 2 MHz, and is ideal for building into function generators and similar instruments, where it gives a far more accurate frequency indication than the traditional frequency dial.

Design by H. Kühne

FREQUENCY scales on sine-wave generators, function generators and pulse generators are usually mechanically coupled, and by no means accurate enough for many applications. Even if the scale is individually calibrated, it is not always easy to accurately set the desired frequency. Not surprisingly, an increasing number of generators is fitted with an internal frequency meter that functions as a frequency scale, or read-out. Today's electronics technology allows this to be achieved fairly easily. However, building a frequency meter into an existing generator can throw up some unexpected problems. Lack of space on the front panel, for instance, may force you to limit the number of display digits (the present circuit has only four). This, in turn, limits the measurement range. The obvious solution to this problem would appear to switch between the ranges. Unfortunately, this is not as easy as it sounds, since free contacts on the generator's range switch are often not available. It is, therefore, better to ensure that the display circuit operates independently from components in the existing instrument.
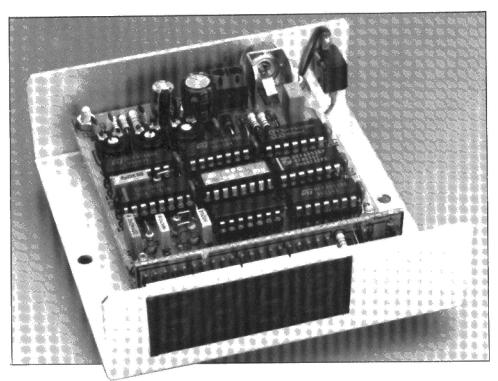
The solution

The usual method of making measurement instruments select the appropriate range is based on the most significant digit (or digits) on the display. If the number is too high, an overflow occurs, and a higher range is selected. If the number is too low, (for instance, nought), a lower range is selected. Obviously, if this system is used, it may take one or several measurements before the right range is found. Apart from the fact that monitoring the most significant digit is troublesome from a point of view of design (frequency meter ICs are not designed for this, so that an extensive decoder is required), the most annoying disadvantage of this method is the slow response to changes in the input signal frequency. Obviously, if you turn the frequency control on a generator, you want to see the set frequency as quickly as possible.

The present circuit uses a different approach. Essentially, it uses the input signal to determine which range is most appropriate. This is achieved by comparing the period of the input signal with three fixed *RC* times. The result of this comparison enables the right range to be selected from the available four. Actually, the comparison between the period time and the *RC* times takes place every other period of the input signal. This enables the circuit to 'know' the input frequency at practically any instant, and to use the value to set the appropriate range at the start of a measurement.

The circuit

The input signal enters the circuit via Schmitt-trigger IC1a. The use of a Schmitt-trigger gate allows sinusoidal and triangular waveforms to be measured alongside rectangular signals. As long as the input signal is greater than 1.7 V_{pp}, the Schmitt-trigger turns it into a neat rectangular wave that can be used by the frequency display without problems. The input signal is first divided by two in bistable IC3a to enable the period to be measured. The output of the bistable is alternately low and high, corresponding to the periods of the input signal. This signal is used to drive the circuit that determines the range selection. The range selection control consists of bistables IC3b, IC4a and IC4b, electronic switches IC8b-IC8d, and the *RC* networks with C2-C3-C4. If the output of IC3a is logic high, the electronic switches are closed, and the three capacitors are discharged. As soon as the output of IC3a goes low, the switches are opened, and the three

capacitors are charged at different rates. Depending on the period of the input signal, none, one, two or three capacitors (C2, C3, C4) are charged until the data input of the bistable connected to each of the capacitors recognizes the voltage level as a logic 'one'. At the end of the period, when the output of IC3a reverts to high, the bistables are supplied with a clock signal that serves to record the charging level of the three capacitors. Finally, the three bistable output signals are

MAIN SPECIFICATIONS

- Four-digit LED display
- Automatic range selection
- Measurement range: 1 Hz - ≥2 MHz
- Accuracy: ±(5 ppm of readout + 1 digit)
- Drift due to ageing: ±3 ppm/ year
- Input sensitivity: 1.7 V_{pp}
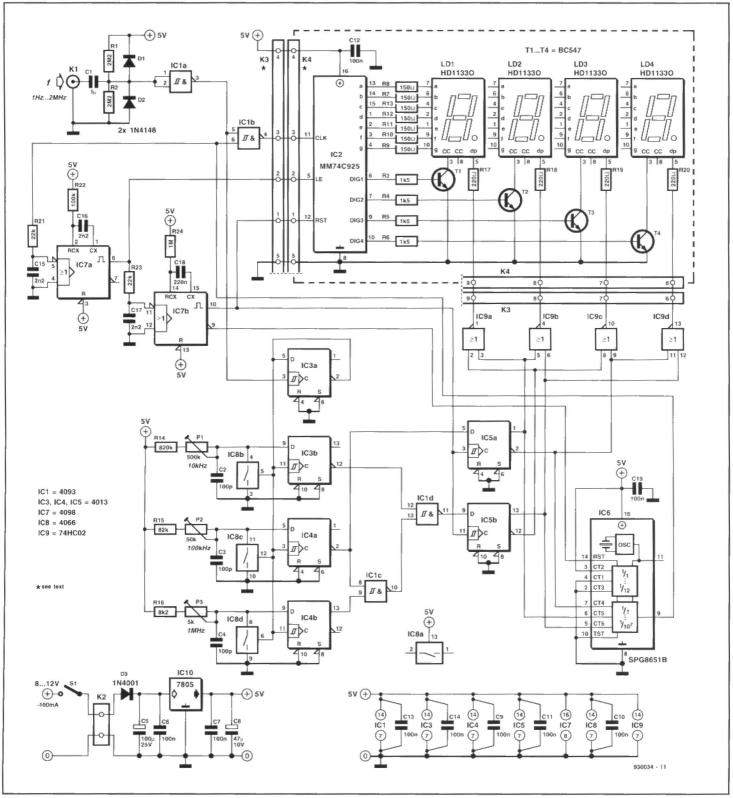
Fig. 1. Circuit diagram of the universal frequency readout.
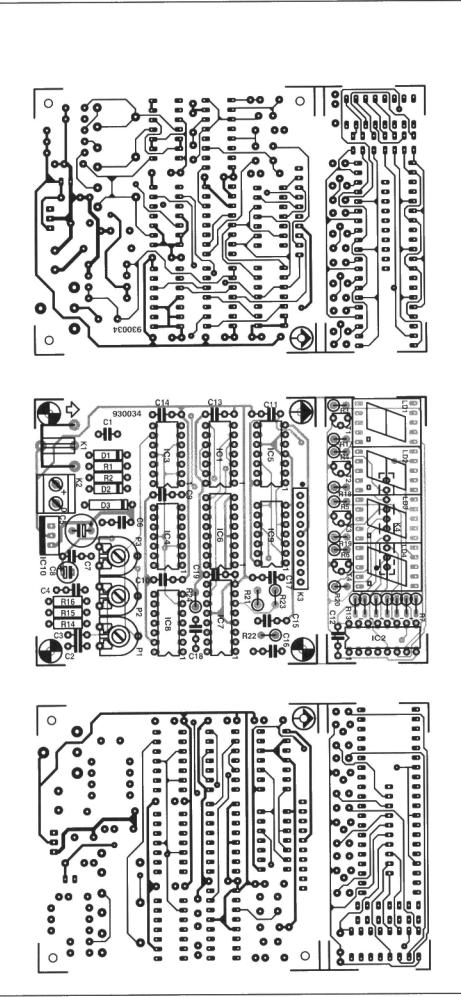
Fig. 2. The double-sided and through-plated printed circuit board consists of two sections to keep the overall size of the readout as small as possible.

COMPONENTS LIST

Resistors:
2	2MΩ2	R1;R2
4	1kΩ5	R3-R6
7	150Ω	R7-R13
1	820kΩ	R14
1	82kΩ	R15
1	8kΩ2	R16
4	220Ω	R17-R20
2	22kΩ	R21;R23
1	100kΩ	R22
1	1MΩ	R24
1	500kΩ preset H	P1
1	50kΩ preset H	P2
1	5kΩ preset H	P3

Capacitors:
1	1µF MKT	C1
3	100pF	C2;C3;C4
1	100µF 25V radial	C5
9	100nF	C6;C7;C9-C14; C19
1	47µF 10V radial	C8
3	2nF2	C15;C16;C17
1	220nF	C18

Semiconductors:
2	1N4148	D1;D2
1	1N4001	D3
4	BC547	T1-T4
1	4093	IC1
1	MM74C925 (National Semiconductor)[1]	IC2
3	4013	IC3;IC4;IC5
1	SPG8651B (Seiko-Epson)[2]	IC6
1	4098	IC7
1	4066	IC8
1	74HC02	IC9
1	7805	IC10
4	HD1133O (Siemens)[3]	LD1-LD4

Miscellaneous:
1 PCB mount cinch socket K1
1 PCB terminal block pitch 5mm K2
1 10-way angled PCB mount pin header plus socket K3
1 on/off switch S1
1 (optional) Enclosure EM10/03 (ESM)[4]
1 Printed circuit board 930034 (see page 70)

[1] Abacus Electronics Ltd. (0635) 33311; ESD Distribution Ltd. (0279) 626777; Farnell Electronic Components Ltd. (0532) 636311; Jermyn Distribution (0732) 740100; Makro Marketing Ltd. (0628) 604422; Thame Components Ltd. (0844) 261188; C-I Electronics (+31) 45 241877; Viewcom Electronics (081) 471 9338.
[2] Abacus Electronics Ltd. (0635) 33311.
[3] ElectroValue (0784) 442253.
[4] Maplin Electronics (0702) 554161.
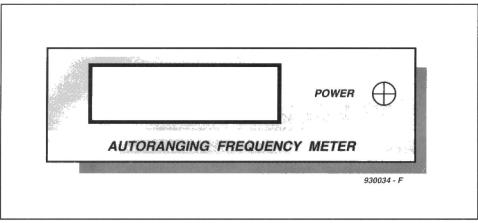
Fig. 3. Suggested front panel design.

combined, by IC1c and IC1d, into two drive signals which are used for the actual range selection.

If the measurement range of a frequency meter has to be changed, the so-called gate time supplied by the time base has to be altered accordingly. The gate time determines how long the frequency meter counts periods of the input signal and, thus, the highest frequency that can be measured. The time base is contained in a single integrated circuit, IC6, which also comprises an accurate quartz crystal oscillator and an adjustable divider. The IC used here, an SPG8651B from Seiko-Epson, was introduced along with a number of other, similar ICs, in an earlier article describing a Mini Square-wave Generator (Ref. 1).

The timebase IC is easily programmed with the aid of the two drive signals furnished by the range recognition circuit. The only proviso is that a measurement once started must not be upset any time the range recognition circuit indicates another range. This is particularly annoying with frequencies close to the range limits. To prevent problems, two bistables are inserted between the range recognition and the timebase control inputs. These bistables, IC5a and IC5b, keep the new data supplied by the range recognition latched until the frequency measurement is started again. The connection between the bistable outputs and IC6 is such that the IC supplies a gate signal of 1 ms (≥1 MHz), 10 ms (100 kHz – 1 MHz), 100 ms (10 kHz – 100 kHz) or 1 s (≤10 kHz), depending on the measurement range required. The outputs of IC5a and IC5b also control the decimal points on the LED display. The points are driven via four NOR gates, IC9a-IC9d, which ensure that the frequency is always displayed in kilohertz (kHz).

The gate time switch is formed by gate IC1b. As long as the gate is open, the input signal arrives at IC2. The MM74C925 contains a four-digit counter, a latch to store the last mea-

surement result, and a multiplexer/display driver to put the measurement result on a readout which consists of four 7-segment LED displays. The external parts around IC2 are limited to seven current limiting resistors for the display segments, and four switching transistors for the multiplex control.

To explain the relation between the various sections of the circuit, a description follows of the events that make up a measurement cycle. The cycle starts and ends with a reset pulse supplied by monostable IC7b. This resets the counter in IC2 and the dividers in timebase IC6. At the same time, the code that represents the last used measurement range is clocked into bistables IC5a and IC5b, and fed to the timebase. After the reset pulse, the time base IC starts to work again. As soon as its output goes high, gate IC1b is enabled, and the input signal allowed to reach counter IC2. The output of IC6 goes low after the measurement time has elapsed. Gate IC1b then blocks the input signal, and IC2 stops counting. The logic low level at the timebase output is delayed briefly by R21-C15, and then used to trigger monostable IC7a. The monostable output pulse causes the state of the counter contained in IC2 to be clocked into the internal latch. After a short delay introduced by an RC network, R23-C17, the negative (trailing) edge of this pulse triggers IC7b, which responds by generating the reset pulse. This closes the measurement cycle.

Power supply consideration

It would be nice if the frequency display could be powered by the equipment into which it is incorporated. Although the supply voltage (if necessary, via IC10) will not be a problem in most cases, the current drain (approx. 100 mA) could be on the high side. If problems are envisaged, it is recommended to power the frequency display

from a mains adaptor. This solution is both economical and safe.

The printed circuit board

The reason for keeping the printed circuit board as small as possible is obvious: the frequency display is intended for incorporating into existing equipment. Not surprisingly, the PCB is double-sided and through-plated. Furthermore, the PCB consists of two sections (display board and main board) which are mounted together at right angles. This reduces the space required for the unit considerably. Obviously, it is also possible to mount the two boards further apart, and interconnect them via a length of flatcable. For the right-angle construction, an angled PCB pinheader is mounted in position K3, and nothing in position K4. If desired, the displays are inserted into a 40-way IC socket. This raises the displays above the other parts, and allows them to be mounted flush against a front panel bezel. When all parts have been mounted on to both PCBs, the pinheader pins are inserted into the holes for K4 on the display board. This connection between the two boards is secure by virtue of the through-plated holes.

Testing
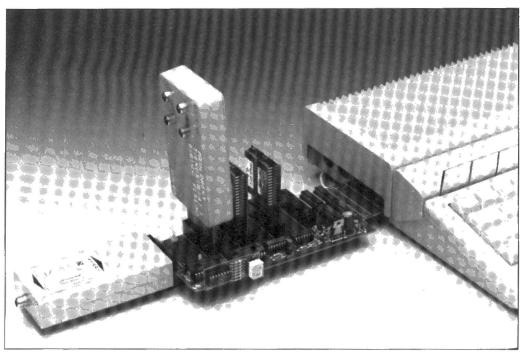
Initially, turn the wipers of the three presets fully anti-clockwise. Next, apply an input signal with a frequency of 9.5 kHz. Monitor the voltage at pin 13 of IC3, and carefully advance P1. The setting is correct when the voltage suddenly goes high. If you have the feeling that P1 is set too far, turn the wiper back, and start again. Next, do the same for P2, at an input frequency of 95 kHz, measuring the voltage at pin 1 of IC4. The last adjustment is P3: input frequency 950 kHz, voltage measured at pin 13 of IC4. That completes the adjustment, since the timebase is factory calibrated. ∎

Reference:
1. Mini Square-wave Generator, *Elektor Electronics* February 1992.

ROM GATE SWITCH-OVER FOR ATARI ST

Many games, utilities and other application software for the Atari ST computer are supplied as ROM/EPROM modules ('cartridges') of which, unfortunately, only one at a time can be connected to the computer. The circuit described here overcomes this undoubted shortcoming of an otherwise excellent computer. It allows up to five ROM/EPROM modules to be connected at the same time, and to be selected by software.

Design by E. Gilissen

THE circuit diagram of the ROM gate switch-over, **Figure 1**, is of an elegant simplicity. It can be functionally divided into four sub-circuits. Firstly, there is the connector that links the unit to the Atari's ROM port. This connector, shown in the upper left-hand corner of the diagram, consists of contact fingers etched on the printed circuit board. Two parallel connectors, K8 and K9, are provided to allow the unit to be connected to the Atari via a cable.

The second block contains the electronics proper, which includes four 8-bit bus transceivers (or bus buffers), IC1 to IC4, and two 4-to-16 line decoders/demultiplexers, IC5 and IC6. Between the bus buffers and the decoders sit a 4-bit 3-state output data latch, and five inverters contained in IC8.

The third block consists of the output connectors, K1 to K5, into which the Atari cartridges are inserted.

The fourth block contains a 7-segment LED display which is driven by a BCD-to-7-segment latch/decoder/driver, IC9. The dashes around this sub-circuit indicates that it forms a separate unit. The 7-segment LED display indicates the number of the cartridge selected by the software.

The switch-over unit and the cartridges connected to it are powered by an inexpensive mains adapter with an (unregulated) output voltage between 8 V and 15 V d.c.

To protect the host computer to which the unit is connected, all bus lines are buffered by 74HCT245 devices. Also, the switch-over unit is powered externally, for instance, by an external disk drive power supply.

Since the data flow is unidirectional (from the switch-over unit to the computer only), the G3 (direction) control inputs of the databus buffers, IC1 and IC2, are normally held at a fixed positive level by resistor R2. The buffers are enabled via their G3 inputs by a low level on the $\overline{ROM3}$ or $\overline{ROM4}$ line. The OR function (for logic low levels) is provided by diodes D3 and D4.

The address bus lines are buffered by IC3 and IC4. Of the 16 buffers available in the two HCT245 devices, 15 are used for the Atari's address lines, and one for the $\overline{ROM3}$ line. Buffering of this line is essential because of the relatively high load on it.

For your reference, the pinning of the Atari cartridge (ROM port) connector is given in **Fig. 2**.

A small modification is required inside the Atari computer. Pin 2 of the ROM port connector is disconnected from the +5 V supply voltage (Vcc), and connected to the PA7 line, which can be taken from pin 14 of the sound generator IC Type AY8910. After this modification, it is no longer possible to connect cartridges to the Atari without making use of the switch-over unit. If you object to this, install a small change-over switch that allows cartridge connector pin 2 to be taken to Vcc or the PA7 line.

How it works

When the circuit is switched on, network R3-C1 resets the four-bit latch, IC7. This results in the circuit starting from 'cartridge 0'. When the PA7 line is made logic high, the output of IC8a enables the HCT173 latch via its G1 input. At the same time, IC5 is disabled by inverter IC8b. When a READ operation is performed in the address range reserved for ROM3 ($FBxxxx), the four least-significant address lines, A1 to A4, are latched on the rising (positive) edge of the $\overline{ROM3}$ signal. Because of the pull-up resistors on the databus lines, the computer reads a dummy value which consists of 'all ones', i.e., $FFFF. Next, by making PA7 logic low, each READ operation in the $\overline{ROM3}$ or $\overline{ROM4}$ address range enables one of the 74HCT154 decoders, which, in turn, translate the 4-bit latched data supplied by IC7 into a corresponding cartridge select signal. The five output signals of each 4-bit binary decoder, $\overline{ROM3.0}$ to $\overline{ROM3.4}$ (IC5),
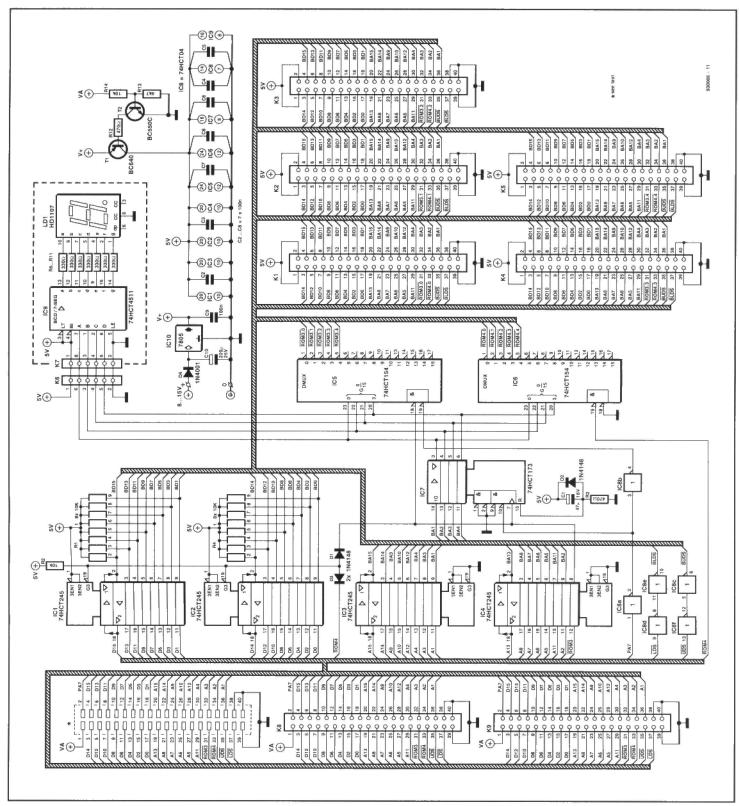
Fig. 1. Circuit diagram of the ROM switch-over for Atari ST computers.

and $\overline{\text{ROM4.0}}$ to $\overline{\text{ROM4.4}}$ (IC6), are taken in pairs to the five cartridge connectors on the board. The cartridge selection is unique, that is, only one cartridge at a time is effectively connected to the Atari host computer.

Inverters IC8d and IC8f buffer the LDS and UDS signals respectively. These signals are found back as BLDS and BUDS on each of the cartridge connectors.

The last part of the circuit to be discussed is the power-on enable switch, T1-T2. The function of this subcircuit is to ensure that the ICs on the switch-over unit are not powered before the Atari computer is switched on. This is achieved by making use of a switching voltage, +VA, taken from pin 1 of the cartridge connector. Likewise, the transistor switch also ensures that the ICs on the switch-over unit are cut off when the Atari is switched off. This happens despite the fact that the power supply of the switch-over unit is still on.

Construction

The printed circuit board for this project is double-sided, through plated, and, fortunately, available ready-made through our Readers Services. The artwork is given in **Fig. 4**. Because of the high density of the tracks on this board, it is not easily reproduced with hobby tools. We therefore strongly recommend buying this board ready-made.

The board consists of two sections:

```
     1  3  5  7  9  11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
     O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O
     O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O  O
     2  4  6  8  10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40
```

1 – +5VDC	20 – Address 15
2 – +5VDC	21 – Address 8
3 – Data 14	22 – Address 14
4 – Data 15	23 – Address 7
5 – Data 12	24 – Address 9
6 – Data 13	25 – Address 6
7 – Data 10	26 – Address 10
8 – Data 11	27 – Address 5
9 – Data 8	28 – Address 12
10 – Data 9	29 – Address 11
11 – Data 6	30 – Address 4
12 – Data 7	31 – ROM Select 3
13 – Data 4	32 – Address 3
14 – Data 5	33 – ROM Select 4
15 – Data 2	34 – Address 2
16 – Data 3	35 – Upper Data Strobe
17 – Data 0	36 – Address 1
18 – Data 1	37 – Lower Data Strobe
19 – Address 13	38...40 – Ground

930005 - 12

Fig. 2. Pinning of the ROM port (also called cartridge port) connector on the Atari ST computer.

main board and display board. These are easily separated by cutting the two pieces of circuit board that hold them together. Next, the four 'humps' on the board sides are removed with a couple of strokes with a file.

Connectors K8 and K9 are optional, since they serve to connect the board to the Atari via a short length of flatcable. This is achieved by cutting the

In GFABASIC:

```
~XBIOS(30,128)                    !enable HCT173 latch.
~PEEK(&HFB0000+(romno%*2)         !dummy read to base address
                                   + (cartridge no.*2).
~XBIOS(29,127)                    !disable HCT173 latch.
```

In MC68000 machine language:

Entry: D0.W = number of port to be enabled

```
asl.w    #1,d0              ;D0 * 2.
move.w   d0,-(a7)           ;save on stack
move.l   #$1E0080,-(a7)     ;parameter + no. xbios.
trap     #14                ;XBIOS.
lea      $FB0000, a0        ;base address.
move.w   4(a7),d0           ;move D0 to XBIOS again.
move.w   0(a0,d0.w),d0      ;dummy read.

move.l   #$1D007F,(a7)      ;clear previous parameters.
trap     #14                ;XBIOS.
addq.w   #6,a7              ;both .W and .L equal to An.
```

Fig. 3. Examples of cartridge selection under software control.

board between K8 and K9, and fitting 40-way pin headers in the connector positions. These headers are linked by a flatcable fitted with a 40-way IDC ('press-on') socket at either end. If remote connection is not required, simply leave the main board whole, and omit K8 and K9.

The first thing to do after separating the display board from the main board is to change four of the five Atari cartridge connectors from angled pin types into straight pin types. The latter are, apparently, not available. Straighten the 40 pins on each connector carefully with the aid of a pair of precision pliers. Obviously, not all five connectors need to be fitted if you never plan to fit five cartridges.

Connector K5 remains an angled pin type to allow cartridges for horizontal mounting to be used, too.

Start the construction with the display board. The LED display is best inserted into a socket made from two 5-pin sockets cut from a longer strip. The display board is mounted at right angles to the main board with the aid of an angled pin header (K6-K7) cut to a length of six pins. If you can not get hold of such a connector, six left over resistor wires, bent at 90°, will do equally well.

The construction of the main board will take a little more time. Start by fitting the small components, i.e., the diodes, resistors, resistor networks, capacitors, the voltage regulator and the transistors. Next, fit sockets for all ICs, taking good care to observe the orientation indicated by the component overlay. Finally, mount the cartridge connectors. Note that these have no PCB orientation notches.

The 3-mm holes in the main board may be used to insert plastic PCB stand-offs that serve to prevent the board from bending downward and exerting strain on the Atari's cartridge connector.

Having completed the switch-over board, you are ready to proceed with the PA7 signal, which is taken from pin 14 of the AY8910 sound generator IC. Several options are available, so read the following carefully.

Solder one end of a 40-cm long wire either directly to pin 14 of the AY8910, or to the corresponding solder island at the track side of the computer's main board. The latter option requires disassembling the computer to gain access to the solder side of the main board.

You then have two options: the PA7 connection may be made (1) via the cartridge connector, or (2) via the wire described above.

For option (1): Cut the track that leads to pin 2 of the cartridge connector in the computer. Reduce the length

of the above mentioned wire as required, and solder the free end to pin 2.

For option (2): Cut the track that starts at contact finger '2' of the etched connector on the main board (contact finger '2' is at the solder side of the board). The cut is made close to the contact finger. Next, connect the free end of the wire to the track that runs close to the edge of the board.

It should be noted that option (1), the 'connector link', is preferred over the 'flying wire' alternative.
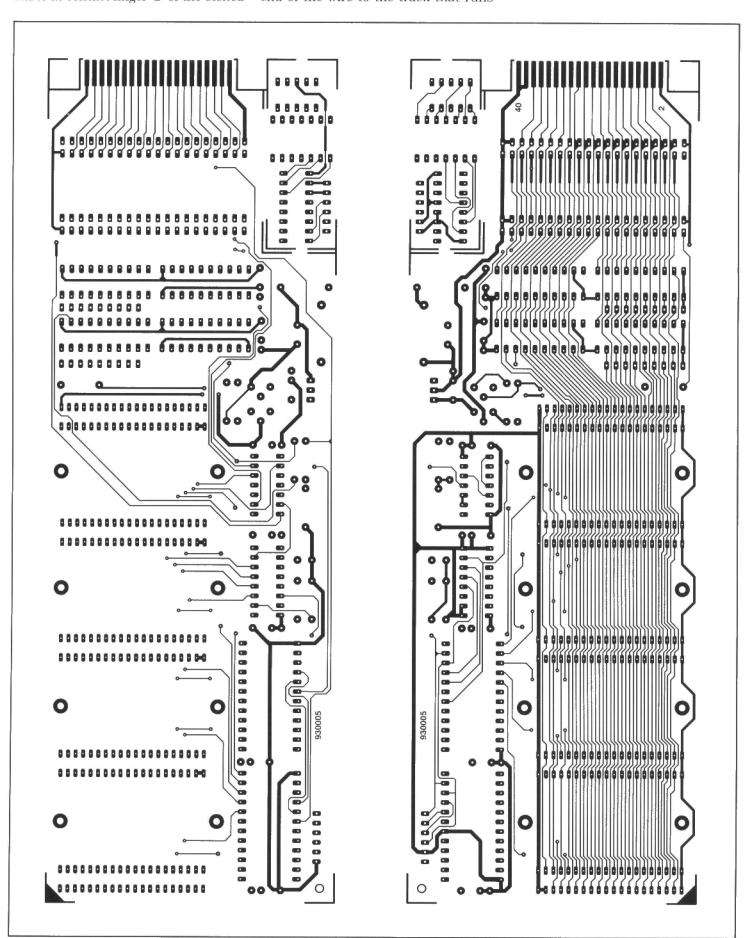
Fig. 4a. Track layouts of the double-sided PCB designed for the ROM switch-over unit.

Testing

Having checked the work so far for short-circuits, cold solder joints and incorrectly orientated parts, it is time to run a few initial tests. Switch off the Atari, and insert the ROM switchover unit into the cartridge connector at the side of the computer. Make sure the PA7 signal is fed to the switchover board — see above for the options.

Switch on the ROM switch-over unit, and then the Atari. If everything goes well, the display should indicate '0', which means that the computer has access to the cartridge inserted into connector K1. Cartridges containing 'boot-up' programs should, therefore, be inserted into K1.

If this works, switch off the Atari, and then the switch-over unit. Next, plug your cartridges on to the connectors on the board. Switch the computer and the switch-over unit on again.

Software

As already mentioned, the cartridge selection runs under software. Either GFA-BASIC or machine code may be used for this purpose, and **Figure 3** gives the 'bare bones' software to get you going. ∎
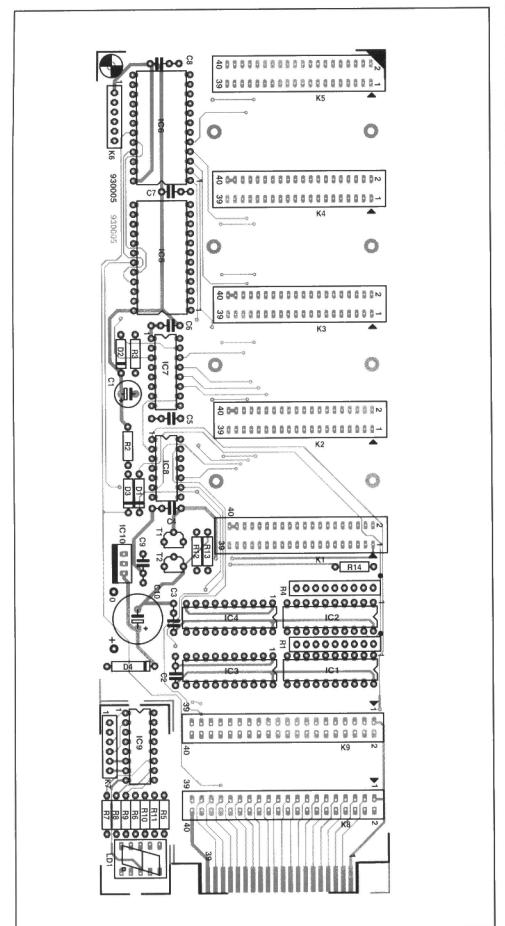
Fig. 4b. Component mounting plan.

COMPONENTS LIST

Resistors:
2	8-way 10kΩ SIL	R1;R4
2	10kΩ	R2;R14
2	470Ω	R3;R12
7	330Ω	R5-R11
1	4kΩ7	R13

Capacitors:
1	47µF 16V radial	C1
8	100nF	C2-C9
1	220µF 25V radial	C10

Semiconductors:
3	1N4148	D1-D3
1	1N4001	D4
1	BC640	T1
1	BC550C	T2
4	74HCT245	IC1-IC4
2	74HCT154	IC5;IC6
1	74HCT173	IC7
1	74HCT04	IC8
1	74HCT4511	IC9
1	7805	IC10
1	HD1107O (Siemens)[1]	LD1

Miscellaneous:
5	Atari 40-way female cardedge connector	K1-K5
1	6-way SIL socket	K6
1	6-way SIL header	K7
2	40-way box header	K8,K9
1	Printed circuit board 930005 (see page 70)	

[1] ElectroValue, Unit 3, Central Trading Estate, Staines, Middlesex TW18 4UX. Telephone: (0784) 442253. Fax: (0784) 460320.

MIDI CHANNEL MONITOR

Design by W. Dunczewski

Communication between electronic musical instruments and between musical instruments and a computer is made possible by MIDI (Musical Instrument Digital Interface). Moreover, many other devices, such as lights, smoke generators, and other 'tools of the trade' can be controlled by this interface. Clearly, MIDI offers the musician a host of new facilities.

Unfortunately, MIDI also has a drawback: the exchange of commands takes place via a few lengths of cable, so that the user cannot see what is happening between the various instruments. As long as everything is all right, that is no problem. When an error occurs, it is quite a job to locate where it originates. In such a situation, the present monitor is a real boon. One of a row of LEDs on its front panel shows at which specific channel each MIDI command is directed.
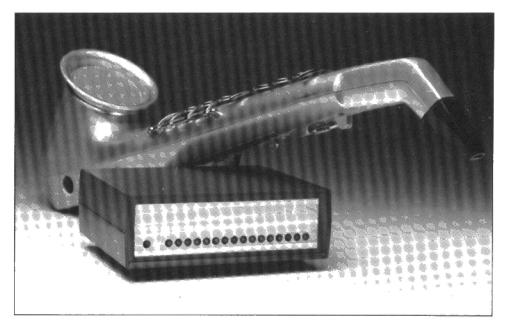
The MIDI channel

As will be gathered from the name MIDI, communication takes place via digital signals. In fact, the entire connection is a simple current loop in which current pulses flow. The data rate at which this happens is 32 kbit sec^{-1}. At the transmitting end, the interface is constructed around an inverting transistor with an open-collector output. At the receiving end, the interface is based on an optoisolator.

Modern electronic musical instruments are often able to generate sound via various channels: for instance, an expander or keyboard can generate sounds simultaneously via several channels. A piano sound may be generated via channel 1 and at the same time the sound of a trumpet via channel 2. In practice, it is thus possible to reach various sounds via one MIDI connection. To ensure that only the wanted sound reacts to the command, the MIDI code has an integral 4-bit address. This means that up to 16 different sounds may be controlled via one MIDI connection. The user has to couple a channel and a sound at the receiving end and connect the correct channel number to the MIDI command. It is here that the present monitor can be a great help.

Broadly speaking, there are four MIDI commands: Channel, System Exclusive, System Real Time and System Common. Only the channel instructions are addressed directly to one sound in an instrument. This is done with an address contained in the code.

System exclusive commands contain a code that refers to the maker and they are normally used to send specific data to an apparatus. This instruction may be used to transfer a complete file from a PC to a musical instrument.

The other two type codes refer to all the equipment that is connected to the MIDI.

There is no doubt that electronics, and particularly the computer, has become a mainstay of much music making. The monitor described in this article is intended primarily for musicians who work regularly with MIDI instruments and computers.

They fulfil functions associated with the synchronization, resetting, starting and stopping the instruments.

Channel commands, which contain data about key strokes and sound selection, are used most frequently.

The monitor indicates by means of 16 LEDs which address has been incorporated in a channel command. The channel instructions that are intercepted for this purpose are:

code	instruction
$8n	note off
$9n	note on
$An	poly key
$Bn	control change
$Cn	programme change
$Dn	channel pressure
$En	pitch wheel

In this table, the 4-bit address code is indicated by n. The monitor examines the data flow at the MIDI connection, detects any channel commands, and extracts the channel number from the code. The associated LED will then be powered.

So as not to waste any connections, there is also a MIDI through-put.

The circuit

The signal from the interface is applied to the circuit (**Fig. 1**) and causes a train of current pulses at the output of optoisolator IC_1. These pulses are reconverted into a MIDI signal via buffers IC_{2e} and IC_{2f}. In other words, K_1-IC_1-IC_{2e}-IC_{2f}-K_2 is the MIDI throughput already referred to.

The current pulses are applied to the remainder of the circuit via IC_{2d} and IC_{2b}. The buffered signal is applied to the D input of IC_5 and to the base of T_1. This transistor ensures that D_3 will light as soon as MIDI data are applied. Circuit IC_5 provides the serial-to-parallel conversion of the 8-bit data. The eight outputs of this IC (pins 4–7 and 11–14) are split into two nibbles. Four bits contain the data on the type instruction; the other four (pins 11–14), give the channel number. The data contained in these latter bits are used by demultiplexer IC_7 to cause one of the 16 LEDs to light via a transistor. The demultiplexer accepts the four bits the instant a pulse is applied to its strobe input (pin 1). This pulse originates from a time base circuit centred on 4 MHz oscillator IC_{2a}, decade counter IC_3, binary counter IC_4 and a few gates. The time base is fairly complex because the measurement time is 9.5 periods. This is unavoidable because the MIDI word contains, apart from the 8 data bits, a start bit and a stop bit. Therefore, when the start bit has been detected, 9.5 periods are needed to receive all data.

The signal at pin 3 of IC_3 is the clock signal divided by 32, while that at pin 151 is the clock frequency divided by 2048. The signal at pin 4 has a frequency of 31.2 kHz. This frequency coincides with the baud rate
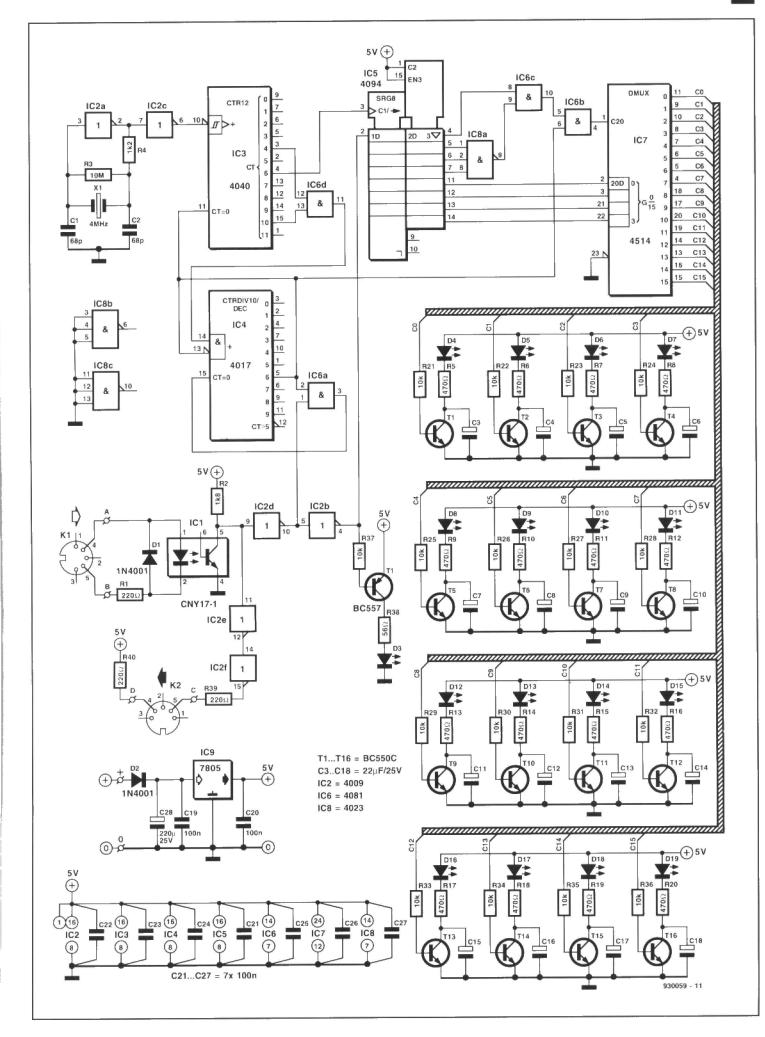
Fig. 1. Circuit diagram of the MIDI channel monitor.
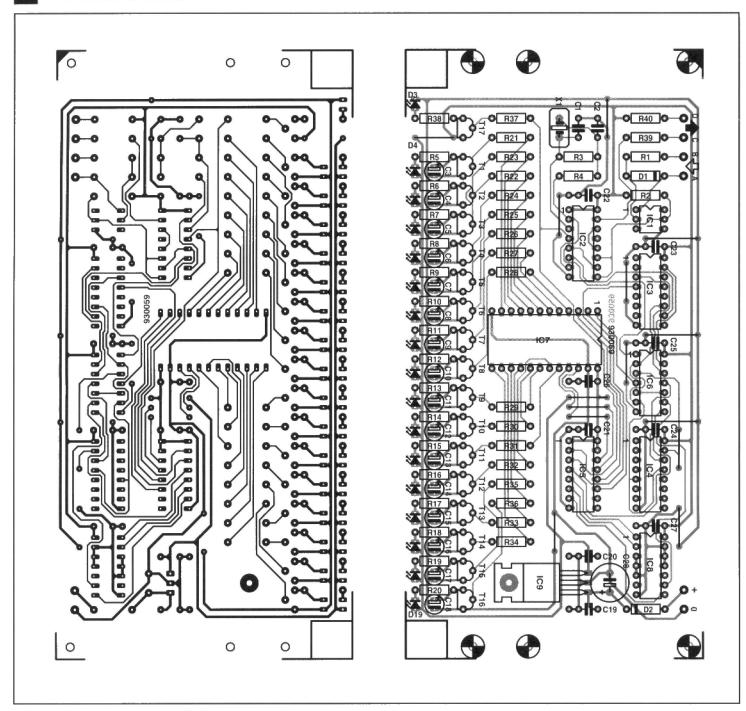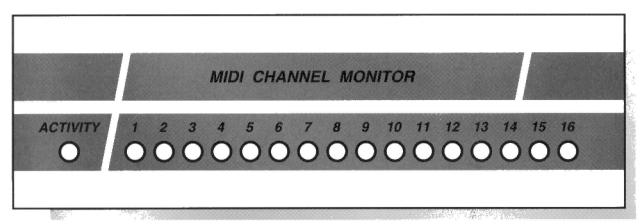
Fig. 2. Printed-circuit board for the MIDI channel monitor.

MIDI CHANNEL MONITOR

ACTIVITY   1   2   3   4   5   6   7   8   9   10   11   12   13   14   15   16

930059 - F

Fig. 3. Suggested front panel for the MIDI channel monitor.

Summary of MIDI codes

Channel

The four highest bits of a channel status byte define the command; the four lowest indicate the channel number.

9x$_H$ **Note ON event**
3 bytes   1001nnnn + 0kkk kkkk + 0vvv vvvv

nnnn
Channel code 0–15 (i.e, 16 channels available)

0kkk kkkk
Key number 0–27
For all keyboards: middle C = 60

0vvv vvvv
Key ON velocity: 0–127
If the keyboard does not contain velocity sensors, 64 is the default value.

8x$_H$ **Note OFF event**
3 bytes   1000nnnn + 0kkk kkkk + 0vvv vvvv

0vvv vvvv
key off velocity

Ax$_H$ **Polyphonic key pressure**
3 bytes   1010nnn + 0kkk kkkk + 0vvv vvvv

0vvv vvvv
Pressure/after-touch value: 0–127
The code is used in the omni mode

Bx$_H$ **Control change**
3 bytes   1011nnnn + 0ccc cccc + 0vvv vvvv

0ccc cccc
Control address: 0–127
Apart from the pitche bender (0), these addresses are not specified

Cx$_H$ **Programme change**
2 bytes   1100nnnn + 0ppp pppp

0ppp pppp
Programme number: 0–127

Dx$_H$ **Channel pressure**
2 bytes   1101nnnn + 0vvv vvvv

0vvv vvvv
Channel pressure/after-touch: 0–127
In mono mode: read key instead of channel

Ex$_H$ **Pitch wheel change**
3 bytes   1110nnnn + 0kkk kkkk + 0vvv vvvv

System exclusive

This command, defined to transmit exclusive instructions, comprises a header of 2 bytes, data bytes and a terminating code of 1 byte.

Format: F0$_H$ + 0iii iiii + data + F7$_H$

F0$_H$
This status byte mustbe followed by an identification code

0iii iiii
Identification code of manufacturer, any value between 0 and 127; some values are Sequential Systems 01$_H$; Kawai 40$_H$; Roland 41$_H$; Korg 42$_H$; Yamaha 43$_H$

data
Any block of data bytes with a value of 0–127 intended for all channels

F7$_H$
This END-OF-BLOCK code terminates the command (which may also be done with a SYSTEM RESET)

System real time

This command enables direct control of the system. Applications are synchronization and rhythm system. System real time commands are transmitted on all channels. Instruments that do not know these commands ignore them.

F8$_H$ **Timing clock in play**
This clock is sent with the transmitter in play mode. The system is synchronized and has a frequency of 24 clock pulses per crotchet (USA: quarter-note)

F9$_H$ **Measure end**
The MEASURE END is sent in place of the TIMING CLOCK IN PLAY at the end of each measure.

FA$_H$ **Start from 1st measure**
This code is sent directly the PLAY key of the master (sequencer or rhythm unit) is pressed. The first TIMING CLOCK IN PLAY must be sent within 5 ms after this command.

FB$_H$ **Continue start**
This code is sent when the CONTINUE knob on the master is used. A sequence is repeated from the point where the latest TIMING CLOCK IN PLAY was received. The next TIMING CLOCK IN PLAY must be sent within 5 ms.

FC$_H$ **Timing clock in end**
This clock is generated when the master is in the wait mode; it is used to lock a PLL (phase-locked loop) in the interval when the PLL must provide the timing.

FE$_H$ **Active sensing**

System common

These data are intended for all instruments on all channels.

F1$_H$ **Undefined**

F2$_H$ **Measure information**
3 bytes   F2$_H$ + 0mmm mmmm (MSB) + 0mmm mmmm (LSB)
The two data bytes code the number of the measure in a 14-bit code.

F3$_H$ **Song select**
2 bytes   F3$_H$ + 0sss ssss
This 7-bit code contains the song number (0–127)

F4$_H$ **Undefined**

F5$_H$ **Undefined**

F6$_H$ **Tune request**
Initializes the voice routines of the synthesizer.

System reset

This command enables the entire system to be reset.

FF$_H$ SYSTEM RESET

of the MIDI signal. This signal is, therefore, used to clock IC_5. The leading edge of the signal coincides with the centre of the MIDI word and is used to sample the data.

The frequency of the signal at pin 15 is $1/16$ of that at pin 4. This means that pin 15 goes high after pin 4 has output 8 pulses. The remaining $1^1/_2$ period is obtained by adding 6 pulses from pin 3 to the half-period at pin 15.

The entire operation is summarized in the timing diagram in **Fig. 5**.
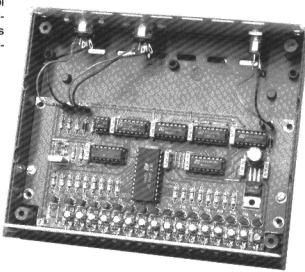
As soon as pins 3 and 15 are high, the output of IC_{6d} also goes high and is used to clock IC_4. At the sixth clock pulse after the reset input has been enabled, pin 5 of IC_4 goes high. At the next leading edge in the MIDI signal, the output of IC_{6a} goes high. Depending on the level at the output of decoder IC_{8a}-IC_{6c}, the clock pulse is passed to IC_7. In practice, this means that when the high nibble of the input MIDI code is $8, $9, $A, $B, $C, $D or $E, the clock pulse is passed to IC_7. All MIDI codes containing an address have then been decoded.

After pin 5 of IC_4 has become logic high, the enable input of this counter is blocked and IC_3 is reset. Circuit IC_4 is reset when the output of IC_{2d} goes high, whereupon a fresh measurement period starts.

As soon as the 4-bit channel code has been stored in IC_7, the output associated with that code will go high. The transistor connected to that output is switched on and the associated LED lights. Since the data often are of very short duration, electrolytic capacitors shunt the transistors. These ensure that the LEDs are quenched slowly to show more clearly which channel was accessed. If the time the LED lights is considered too short, the value of the capacitor may be enlarged up to 220 μF.

The power supply, derived from a mains adaptor (7.5–20 V) is straightforward: D_2 protects against reverse polarity and IC_9

Fig. 4. This inside view of the MIDI channel monitor shows the layout of the board and the various connectors as well as the inter-wiring.

holds the supply voltage at 5 V.

Construction

The monitor is best built on the printed-circuit board in **Fig. 2**. First connect the wire bridges, followed by the passive components. After the LEDs have been soldered into place, bend them at right angles so that they can protrude nicely through the holes in the front panel. It is, of course, good practice to ensure that the height of all LEDs above the board is the same.

Normally, IC_9 does not need to be cooled and can be mounted directly on to the board. After the other ICs have also been soldered into place, fit the board in a suitable enclosure. **Figure 4** shows the construction of the prototype.

After the board has been fitted into the enclosure, wire up the two DIN connectors as shown in **Fig. 1**.

Finally, mount two terminals at the rear of the enclosure for the input from the mains adaptor. Connect these internally to the supply pins on the board (0 and +)

and externally to the mains adaptor.

Link the monitor into a MIDI connection, connect the mains adaptor to the mains, and press one of the keys of the muscial instrument. If everything is all right, one of the 16 LEDs will light to show via which channel the communication took place.

END

PARTS LIST

Resistors:
R_1, R_{39}, R_{40} = 220 Ω
R_2 = 1.8 kΩ
R_3 = 10 MΩ
R_4 = 1.2 kΩ
R_5–R_{20} = 470 Ω
R_{21}–R_{37} = 10 kΩ
R_{38} = 56 Ω

Capacitors:
C_1, C_2 = 68 pF
C_3–C_{18}; C_{28} = 22 μF, 25 V, radial
C_{19}–C_{27} = 100 nF

Semiconductors:
D_1, D_2 = 1N4001
D_3 = LED, red, high efficiency
D_4–D_{19} = LED, green
T_1–T_{16} = BC550C
T_{17} = BC557

Integrated circuits:
IC_1 = CNY17-1
IC_2 = 4009
IC_3 = 4040
IC_4 = 4017
IC_5 = 4094
IC_6 = 4081
IC_7 = 4514
IC_8 = 4023
IC_9 = 7805

Miscellaneous:
K_1, K_2 = 5-way DIN connector for board mounting
X_1 = crystal, 4 MHz
Enclosure as required
PCB No. 930059 (see page 70)

strobe
IC7 (pin1)

clock input
IC4 (pin14)

clock input
IC5 (pin3)

MIDI - data
IC5 (pin2)

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Fig. 5. Timing diagram of the MIDI channel monitor.

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